PROGRAMLANABİLİR GÜÇ KAYNAĞI

Can ÖZDEMİR

Yüksek Lisans Tezi
Elektrik Elektronik Mühendisliği
Anabilim Dalı

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Anadolu Üniversitesi
Fen Bilimleri Enstitüsü
Lisanüstü Yönetmeliği Uyarınca
Elektrik Elektronik Mühendisliği Anabilim Dalı
Elektronik Bilim Dalında
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Olarak Hazırlanmıştır.

Danışman: Prof. Dr. Atila BARKANA

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.5./.9.../.9.1.

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Enstitü Müdürü

İÇİNDEKİLER

İÇİNDEKİLER (devam)

ÖZET

Bu tez çalışmasında elektronik sistemlerin test ve kalibrasyonunda kullanılabilecek bir programlanabilir güç kaynağı tasarlanmış ve gerçekleştirilmiştir. Cihaz, 0 V ile 24 V arası 100 mV aralıklarla ±100 mV hassasiyetle programlanabilmektedir. Cihaz çıkışından maksimum 5 A akım verebilecek güçtedir. Gerçekleştirilen cihazda çıkışın programlanan değerlerde kalıp kalmadığı çalışması sırasında kontrol altında tutulmaktadır. Kullanıcıyla sistem arasındaki iletişim 16 tuştan oluşan bir tuş takımı ve herbir satırına 16 karakter yazılabilen 2 satırlık bir LCD gösterge ile sağlanmaktadır.

Anahtar Sözcükler:

Programlanabilir güç kaynağı
Güç kaynağı
Regülatör

SUMMARY

In this thesis, a programmable power supply which may be used to test and calibrate electronic systems is designed and realized. It can be programmed between 0 V and 24 V with 100 mV steps and ±100 mV tolerance. It has a maximum output current of 5 A. The output is controlled during operation to check whether it is in between the desired limits or not. Communication between the power supply and user is done by a keyboard with 16 keys and a LCD with 2 lines, 16 characters per line.

Key Words :

Programmable power supply
Power supply
Regulator

TEŞEKKÜR

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ŞEKİLLER DİZİNİ

TANIMLAR DIZINI

RAM (Random Access Memory) : Rastgele erişimli bellek.

EPROM (Erasable Programmable Read Only Memory) : Silinebilir, programlanabilir salt okunabilir bellek.

DAC (Digital Analog Converter) : Sayısal veriyi analog voltaja çevirici.

ADC (Analog Digital Converter): Analog voltajı sayısal veriye çevirici.

LCD (Liquid Crystal Display) : Sıvı kristal gösterge.

PIO (Paralel Input/Output) : Paralel giriş/çıkış.

SIO (Serial Input/output) : Seri giriş/çıkış.

1. GIRIŞ

Günümüzün modern elektronik donanımları, sabit iyi regüle edilmiş doğru akım güç kaynaklarına gereksinim duyarlar. Bu gereksinim ya kimyasal enerjiyi elektrik enerjisine çeviren piller ya da dalgalı akım üreteçlerinin ürettiği enerjinin doğru akıma çevrilmesiyle karşılanır. İkinci tür kaynaklardan yüksek güç elde edilebilir ancak akım ve gerilim karakteristikleri, regülasyon yüzdeleri ve gürültü istenen seviyelerde olmalıdır.

Kompleks kartların test edilmesinde farklı anlarda farklı gerilimlere gereksinim duyulmakta ve test işlemi bir bilgisayar kontrolu altında gerçekleşmektedir. Bunun için çıkışı istenen değerlere programlanabilir güç kaynaklarına ihtiyaç vardır.

Programlanabilir güç kaynağı, mantık devreleri ve elektronik devrelerden oluşur. Güç kaynağı çıkışının bir değere programlanması ve bunun kontrol altında tutulması mantık devreleriyle gerçekleştirilir. Güç kaynağından elde edilebilecek güç, elektronik çıkış katının teknik özelliklerine bağlıdır.

Programlanabilir güç kaynakları bilgisayar destekli test sistemlerinde ve çeşitli kalibrasyon işlerinde kullanılmaktadır.

2. LINEER DOGRU AKIM GÜÇ KAYNAKLARI *

Genelde bütün elektronik donanımlar güçlerini bir doğru akım kaynağından alırlar.

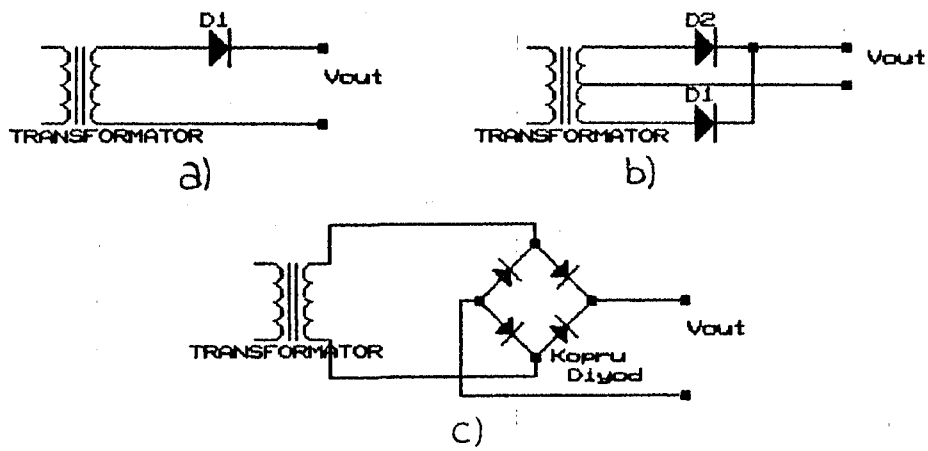
Lineer doğru akım güç kaynakları en az üç kısımdan oluşurlar; transformatör, doğrultucu ve filtre. Güç kaynağı çıkışının daha hassas olması istenen durumlarda çıkışa bir regülatör eklenir.

2.1. Transformatör

Transformatör, kaynağı güç hattından izole ederek giriş voltajını (220 V AC) istenen alçak seviyeye düşürür. Transformatör seçimi, düşürmesi istenen gerilim seviyesine, kullanılacak doğrultucu tipine ve elde edilmek istenen güce göre yapılır.

2.2. Doğrultucu

Alternatif akımı doğru akıma çevirir ve filtre kapasitörün dolma akımı gereksinimini karşılar. Bir veya daha fazla diyoddan oluşur. Devre yapısına göre çıkışında tam dalga veya yarım dalga elde edilir ve bu dalga şekillerine göre isim alırlar (Şekil 2.1.).



Şekil 2.1. Doğrultucu tipleri; a)Yarım dalga, b)Tam dalga, c)Tam dalga köprü doğrultucu.

Yarım dalga doğrultucular genelde düşük akım veya yüksek frekans uygulamalarında kullanılır. Diğer uygulama-

larda genelde tam dalga doğrultucular tercih edilir. Çünkü aynı çalışma frekansı ve ripple voltajı için yarım dalga doğrultucuda iki kat daha büyük filtre kapasitör gereklidir.

Doğrultma işlemi sırasında diyodlar üzerinde 0,6 V ile 1,1 V arası gerilim düşümü meydana gelir. Buna göre devrenin yapısına bağlı olarak bir veya iki diyod üzerinde düşecek gerilim tasarımda göz önüne alınmalıdır. Tam dalga köprü doğrultucuda her zaman iki diyod seri durumdadır. 2,2 V luk kayıp meydana gelir. Bu değer, hesaplamalarda ihmal edilemeyecek kadar büyüktür.

2.3. Filtre

Kapasitansı çekilecek akıma göre belirlenmiş bir kapasitörden oluşur. Görevi, dolma-boşalma periyodlarında çıkışındaki gerilimi yeterli seviyede tutmaktır. Diyodlar iletimde olduğunda kapasitör, bir dahaki dolma periyoduna kadar çıkışı aynı seviyede tutacak yeterli enerjiyi depolar. Tam dalga doğrultucu kullanıldığında 50 Hz lik bir hat sinyaliyle doğrultucu çıkışında 100 Hz elde edilir. Bu durumda kapasitör 10 ms de dolmalıdır ve çıkışı 10 ms yeterli seviyede tutmalıdır.

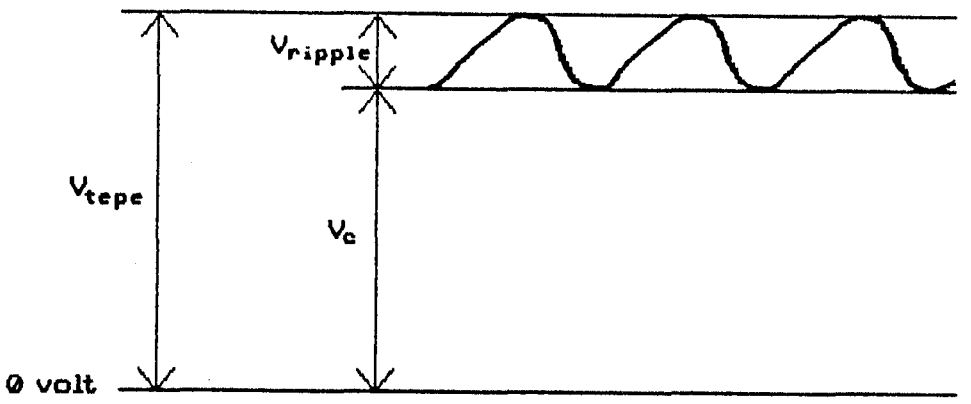
Kapasitörün dolması-boşalması sırasında oluşan dalganın tepeden tepeye değerine ripple voltajı denir (Şekil 2.2.). Güç kaynağında kullanılacak filtre kapasitör değeri Eşitlik 2.1'e göre hesaplanır:

$$C = (T_C / V_{ripple}) \times I \qquad (2.1)$$

Burada C farad biriminde kapasitans, T_C kapasitörün dolma süresi (10 ms), V_{ripple}, izin verilen ripple voltajıdır.

2.4. Voltaj Regülatörü

Voltaj regülatörünün görevi çıkış voltajını önceden belirlenmiş değerde sabit tutmaktır. Çıkış voltajının değişimine neden olan faktörler, yük akımı değişimleri, giriş



Şekil 2.2. Tepe voltajı ve bileşenleri

gerilimi değişimleri ve sıcaklık değişimleridir. Regülatör, bu üç faktörden dolayı meydana gelebilecek çıkış voltajı değişimlerini engellemeye çalışır.

Çıkış voltajının yük akımıyla değişimi yük regülasyonu olarak adlandırılır ve çıkış voltajının yüzdesi olarak ifade edilir. Yük regülasyonu genel formülü

$$(\%) \text{ yük regülasyonu} = \frac{V_{ml} - V_{fl}}{V_o} \times 100 \qquad (2.2)$$

şeklindedir. Burada

V_{ml} : minimum yükte çıkış gerilimi,

V_{fl} : maksimum yükte çıkış gerilimi,

V_o : nominal çıkış gerilimidir.

Giriş regülasyonu ise giriş voltajı değişimlerinin çıkış voltajı üzerine etkisidir. Bu regülasyon çoğu zaman hat regülasyonu diye adlandırılır.

Giriş regülasyonu genel formülü

$$(\%/V_{in}) \text{ giriş regülasyonu} = \frac{\Delta V_o}{\Delta V_{in} \times V_o} \times 100 \qquad (2.3)$$

şeklindedir. Burada

ΔV_o : çıkış voltajı değişimi,

ΔV_{in} : giriş voltajı değişimi,

V_o : nominal çıkış gerilimidir.

Çıkış voltajı sıcaklık sabiti ise sıcaklık değişimleriyle çıkış voltajında meydana gelecek değişim yüzdesidir.

$$(\%/\ C)TC_{Vo} = \frac{\pm(V_{o(max)} - V_{o(min)}) \times 100}{V_{o(ref)} \times (T_{max} - T_{min})} \qquad (2.4)$$

şeklindedir. Burada

$V_{o(max)}$: maksimum sıcaklık (T_{max})'de çıkış voltajı,

$V_{o(min)}$: minimum sıcaklık (T_{min})'de çıkış voltajı,

$V_{o(ref)}$: nominal çıkış voltajı (genelde 25 C'de),

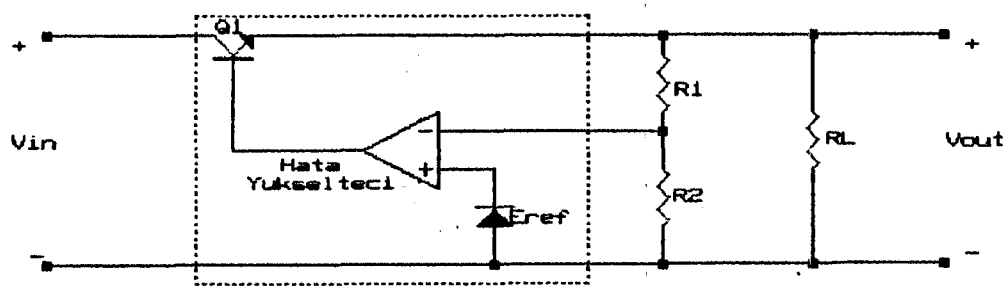
T_{max} : maksimum çalışma sıcaklığı,

T_{min} : minimum çalışma sıcaklığıdır.

Temelde iki çeşit regülatör vardır: seri ve paralel. Seri voltaj regülatörleri değişken yüke sabit voltaj sağlamak için kullanılır. Paralel regülatörler ise sabit yüke sabit voltaj sağlamak için kullanılır.

Bir voltaj regülatörü çıkıştaki değişimleri düzeltmek için bir hata veya fark sinyali üretir. Referans ile regüle edilmiş çıkış voltajının bir kısmı arasındaki fark yükselteç tarafından yükseltilir. Kontrol devresi yükseltilen farkı ve fazını sezerek çıkış voltajını düzeltir.

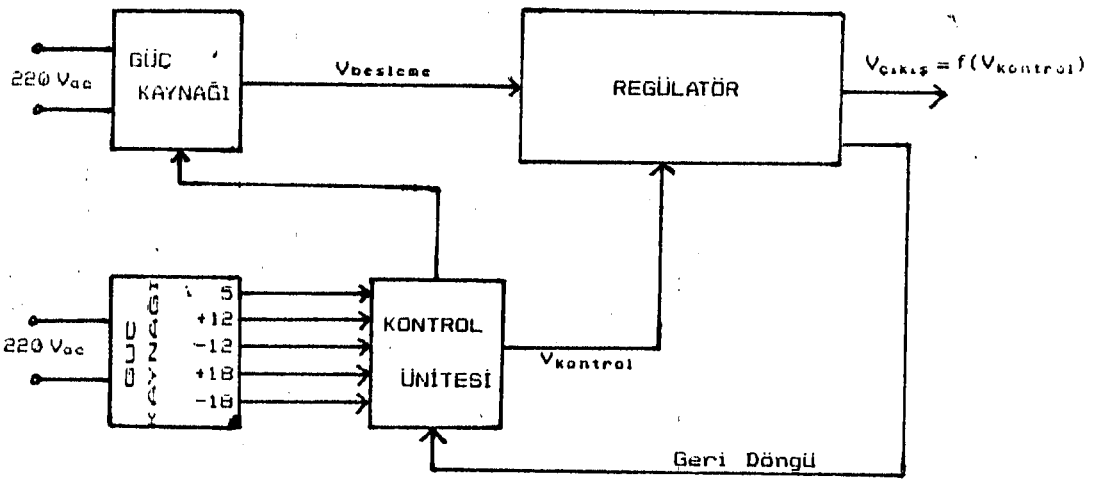
Tipik seri regülatör tümleşik devresi Şekil 2.3'deki gibidir. Tümleşik devre içinde referans voltajı bir zener diyod tarafından üretilir. Tümleşik devre dışına yerleştirilecek bir gerilim bölücüyle (R_1, R_2 dirençleri) çıkış voltajının bir bölümü hata yükseltecine uygulanır. Hata yükselteci giriş ile çıkış arasına seri bağlı transistör üzerindeki gerilim düşümünü kontrol eder.



Şekil 2.3. Tipik seri voltaj regülatörü

3. DONANIM

Sistem dört ana kısımdan oluşur. Bunlar iki ana güç kaynağı, kontrol ünitesi ve regülatördür (Şekil 3.1.).



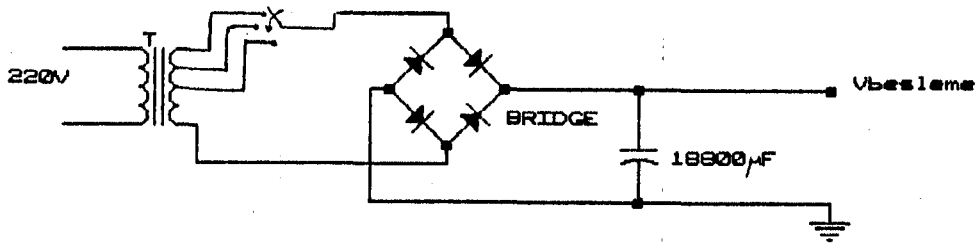
Şekil 3.1. Sistem blok şeması

Kontrol ünitesi, bir mikroişlemci kartı ve mikroişlemci ile diğer analog kısımlar arasında bilgi alışverişini sağlayacak uygunlaştırıcı devrelerinden oluşur. Bu ünite tarafından üretilen $V_{kontrol}$ sinyali çıkış gerilimini istenen değere ayarlar. Ayrıca bir geri döngüyle sistem çıkışı kontrol altında tutulur.Regülatör ünitesi, $V_{kontrol}$ sinyaline göre $V_{çıkış}$ gerilimini üretir.

3.1. Güç Kaynağı

Sistemin güç kaynağı kısmı bütün sistem için gerekli olan gücü üretir. Bu sistem iki ayrı kısımdan oluşur. Bunlardan biri, asıl programlanabilir gerilim kaynağına güç sağlayan yüksek akım çekilebilen kısım, diğeri de kontrol sistemlerine güç sağlayan kısımdır.

Yüksek akım çekilebilen, programlanabilir güç kaynağının çıkışını besleyen kısımda hat gerilimini alçak seviyelere düşüren çok uçlu bir transformatör, tam dalga doğrultucu ve filtre kapasitör vardır.



Şekil 3.2. 30 V güç kaynağı

Programlanabilir güç kaynağı çıkışından elde edilmek istenen gerilim seviyesine göre transformatör çıkışlarından 12 V_{ef}, 18 V_{ef} veya 24 V_{ef} ten biri seçilir. Bu durum göz önüne alınarak güç kaynağında çok uçlu ve yüksek güçlü bir transformatör kullanılmıştır.

Transformatörden sonra gelen tam dalga doğrultucu girişindeki sinüsoidal işareti doğrultarak filtre kapasitörlerine gerekli akımı sağlar. Tam dalga doğrultucudan sonra yer alan filtre kapasitör, diyodların iletimde ve kesimde olduğu anlarda çıkışındaki gerilimi sabit düzeyde tutar. Kaynaktan çekilecek akıma göre dolma ve boşalma sürelerinin hesaplanarak kapasitör değerlerinin buna göre bulunması gerekir (Bakınız Bölüm 2).

V_c = 30 V_{ac} (Kaynak çıkışında istenen gerilim)

V_{ripple} = 2,5 V (Tepeden tepeye periyodik dolma-boşalma gerilimi)

$V_{tepe} = V_c + V_{ripple} = 30 + 2,5 = 32,5$ V

I_{out} = 5 A (Maksimum çıkış akımı)

V_{rect} = 2,2 V (Doğrultucu diyodlar üzerindeki gerilim düşümü)

$$T_c = \frac{1}{2x50\ Hz} = 0,01\ sn$$

$$C = \frac{T_c}{V_{ripple}} \times I = \frac{10x10^{-3}\ sn}{2,5\ V} \times 5\ A = 20\ mF$$

20 mF değerini elde etmek için 4 adet 4700 µF 40 V luk elektrolitik kapasitör kullanılmıştır.

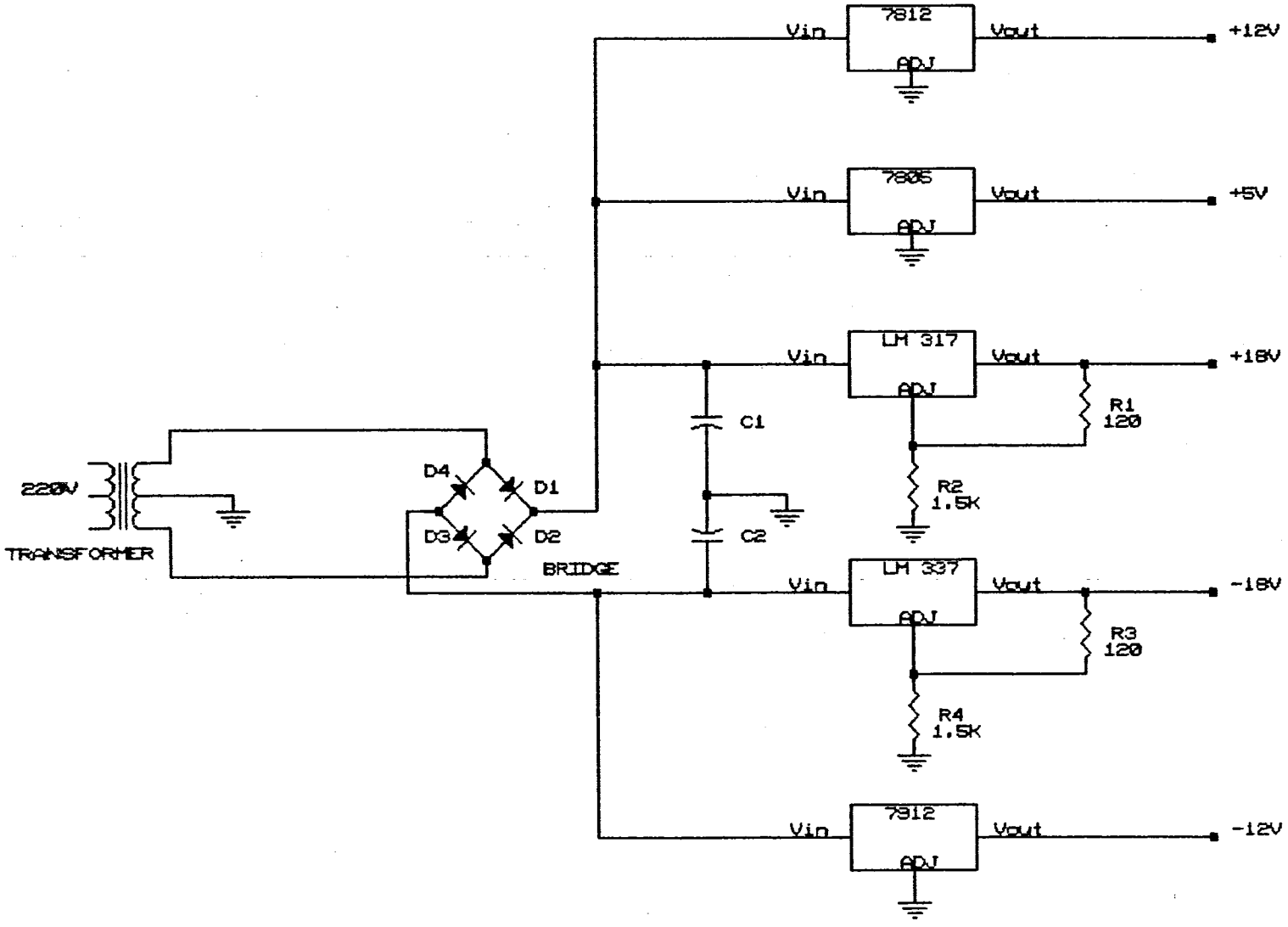
Kontrol sistemlerine güç sağlayan diğer kısım ise gene aynı şekilde transformatör, tam dalga doğrultucu, filtre kapasitör ve regülatörleri içerir. Sistem çıkışından +5 V, ±12 V, ±18 V gerilimler verecek şekilde tasarlanmıştır (Şekil 3.3.).

3.2. Regülatör (LM338)

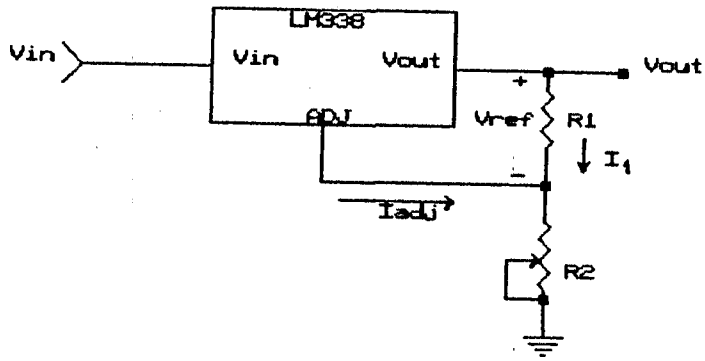
Sistemin bu bölümünde güç kaynağı tarafından üretilen sabit $V_{besleme}$ gerilimi, kontrol sistemi tarafından üretilen kontrol gerilimi ile istenilen değere ayarlanır.

Programlanabilir güç kaynağının çıkışında hem iyi bir regülasyon sağlamak, hem de üreteç çıkışını programlanan değere ayarlayabilmek için LM338, üç bacaklı, ayarlanabilir gerilim regülatörü kullanılmıştır. LM338 entegresinin seçilmiş olmasının başlıca nedenleri ayarlanabilir olması ve çalışma aralığının (gerilim ve akım) amaca uygun olmasıdır. LM338 1,2 V - 32 V arası 5 A çıkış verebilen bir voltaj regülatörüdür. Normal olarak iki direnç ile çıkış gerilimi istenilen değere ayarlanabilmektedir. Çok iyi yük ve hat regülasyonu sağlar (sırasıyla %0.1 ve %0.05/V). Entegrede yer alan akım sınırlama devresiyle kısa süre için 12 A'e kadar akım çekilebilir. Bu tam yük altında sistemin ilk açılışını ve geçici yük değişimlerinde sistemin kullanılabilmesini sağlar. Ayrıca entegrede fazla sıcaklık yüküne karşı koruma (Thermal overload protection) vardır. LM338 entegresi ile ilgili daha geniş bilgi EK.1' de sunulmuştur.

Çalışması sırasında LM338 "V_{out}" çıkışı ile "Adj" çıkışı arasında 1,25 V luk nominal gerilim üretir. Bu sabit gerilim R_1 direnci üzerinde gözlenir (V_{ref}) ve bu direnç üzerinden I_1 sabit akımı akar.



Şekil 3.3. Kontrol sistemleri güç kaynağı



Şekil 3.4. LM 338 tipik uygulama devresi

LM338 de çıkış geriliminin ifadesi:

$$V_{out} = V_{ref} + (I_1 + I_{adj}) \times R_2$$

burada $I_1 = \frac{V_{ref}}{R_1}$ dir.

$$V_{out} = V_{ref} + \left(\frac{V_{ref}}{R_1} + I_{adj}\right) \times R_2$$

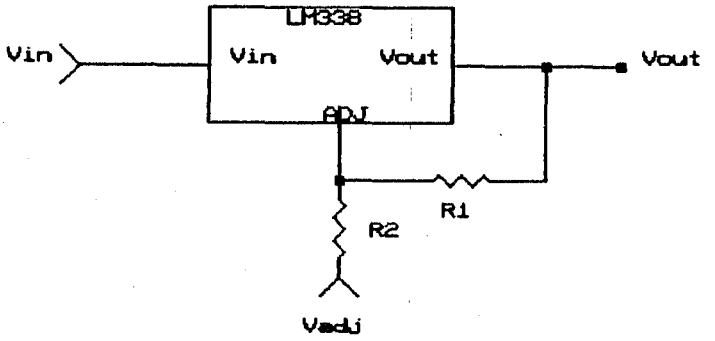
$$V_{out} = V_{ref} \times \left(1 + \frac{R_2}{R_1} \right) + I_{adj} \times R_2 \qquad (3.1)$$

LM338 entegresi I_{adj} akımını minimize edecek ve yük değişimleriyle bu akımı sabit tutacak şekilde tasarlanmıştır.

3.3. Regülatör Çıkış Geriliminin Nümerik Olarak Ayarlanması

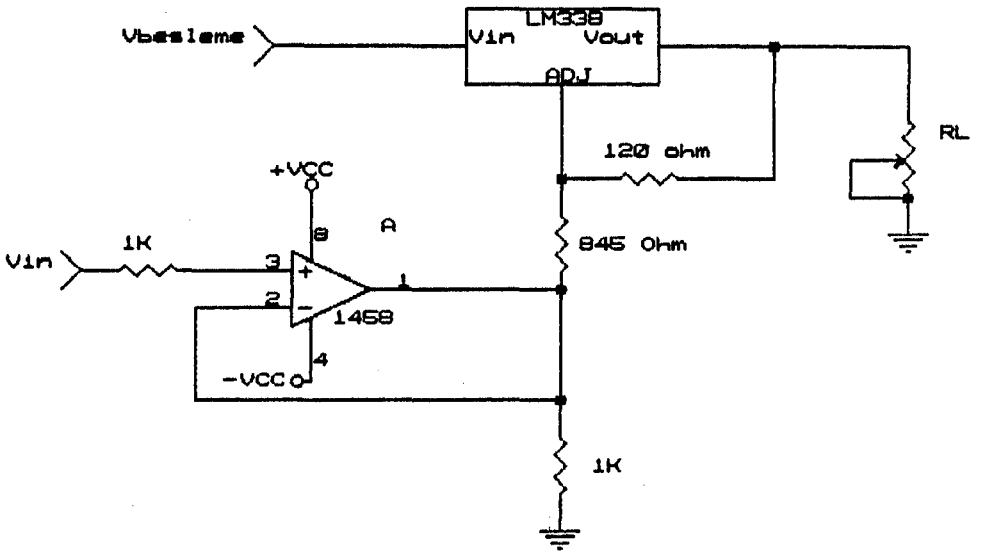
Şekil 3.4 ' deki tipik uygulama devresinde R_1 direnci sabit tutulup R_2 direnci değiştirilerek çıkış gerilimi 1,2 V ile 32 V arasında ayarlanabilir. Eğer R_2 direncini de sabit tutar, Şekil 3.5' deki gibi bu dirence seri bir gerilim kaynağı bağlanırsa çıkış ifadesi direk olarak bu kaynak gerilimine bağlı kalır.

$$V_{out} = V_{ref} \times \left(1 + \frac{R_2}{R_1}\right) + I_{adj} \times R_2 + V_{adj} \qquad (3.2)$$



Şekil 3.5. Çıkış geriliminin V_{adj} gerilimi ile değiştirilmesi

V_{adj} gerilimi Şekil 3.6' daki gibi bir işlemsel kuvvetlendirici üzerinden R_2 direncine uygulandığında V_{adj} gerilimi ile V_{out} çıkış gerilimi arasında Şekil 3.7' de görüldüğü gibi lineer bir ilişki gözlenir.



Şekil 3.6. Çıkış geriliminin V_{in} gerilimi ile değiştirilmesi

V_{adj} ile V_{out} arasındaki bağıntıyı şu şekilde çıkartabiliriz:

V_{ref} = 1,25 V, R_1 = 120 Ω, R_2 = 845 Ω, I_{adj} = 40 μA için

$$I_1 = \frac{V_{ref}}{R_1} = \frac{1,25}{120} = 10,42 \text{ mA}$$

$$I_2 = I_1 + I_{adj} = 10,42 \text{ mA} + 40 \text{ µA} = 10,46 \text{ mA}$$

$$V_{out} = V_{ref} + I_2 \times R_2 + V_{in}$$

$$V_{out} = 1,25 + 10,46 \times 10^{-3} \times 845 + V_{in}$$

$$V_{out} = V_{in} + 10,089 \qquad (3.3)$$

Şekil 3.6' daki devre üzerinden 45 adet V_{in} gerilim seviyesine karşılık ölçülen V_{out} değerleri (çizelge 3.1) ile V_{out} - V_{in} grafiği çizilmiştir (Şekil 3.7.). Lineer regresyon yöntemiyle grafikte elde edilen doğrunun matematiksel ifadesi çıkartılmıştır.

$$V_{out} = a \times V_{in} + b$$

$$b = \frac{\Sigma x . \Sigma y}{n\Sigma x - (\Sigma x)}$$

$$a = \frac{\Sigma y}{n} - \frac{b . \Sigma x}{n}$$

$$a = 0,99829$$

$$b = 10,1374$$

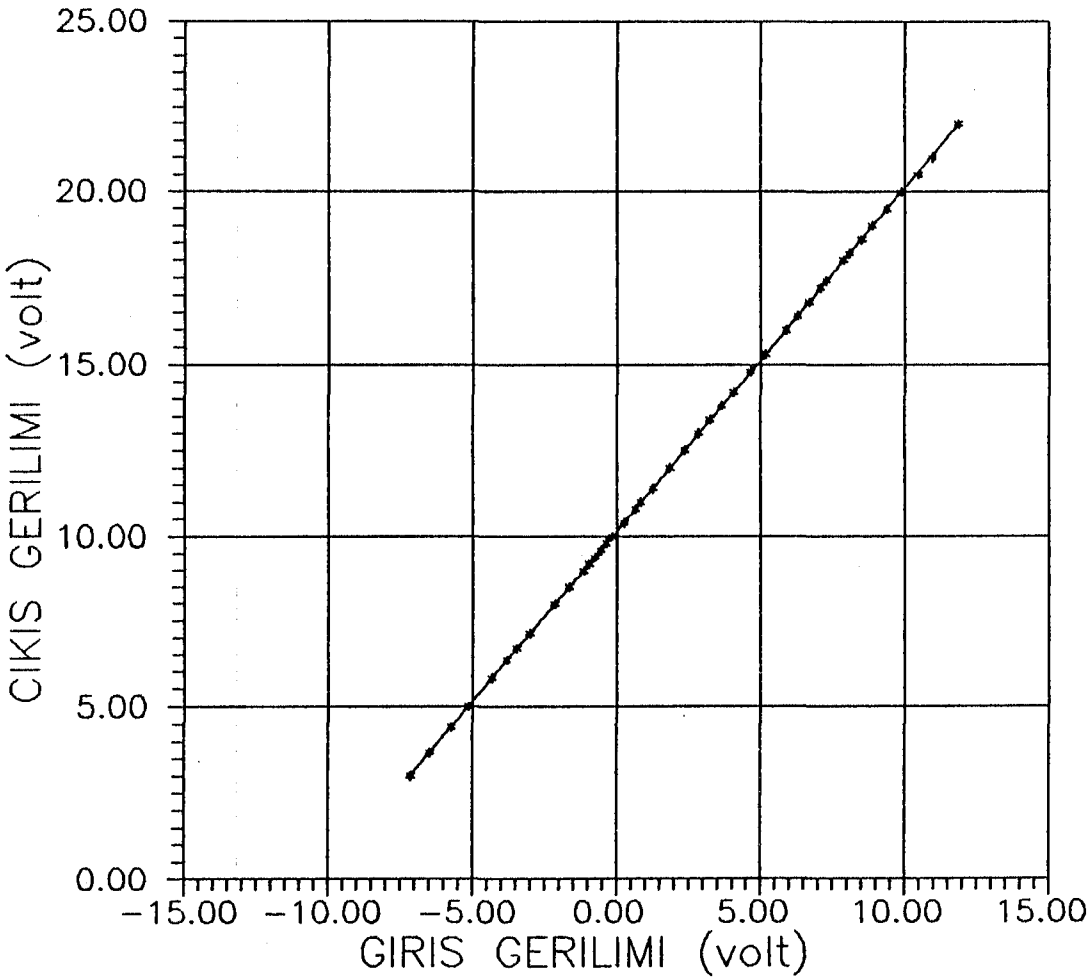
$$V_{out} = 0,99829 \times V_{in} + 10,1374 \qquad (3.4)$$

Elde edilen (3.4) eşitliği V_{out} çıkış geriliminin işlemsel kuvvetlendiricinin "+" girişine uygulanacak V_{in} gerilimiyle hassas bir şekilde ayarlanabileceğini göstermiştir. Bu sonuçtan hareketle V_{in} geriliminin nümerik olarak değişimini sağlayarak V_{out} çıkış geriliminin nümerik değerlerle bir mikroişlemci tarafından kontrolu yoluna gidilmiştir. Mikroişlemci sistemi ve ayarlama geriliminin (V_{in}) uygulandığı işlemsel kuvvetlendirici arasına Digital/Analog Converter (DAC) yerleştirilmiştir. DAC, girişine uygulanan nümerik bilgiyle doğru orantılı akım üretmektedir. Üretilen akım gerilime çevrilerek V_{in} gerilimi olarak devreye uygulanmaktadır.

No	Vin Volt	Vout Volt
1	-9,93	0,235
2	-9,09	1,06
3	-8,70	1,45
4	-8,14	2,00
5	-7,72	2,41
6	-7,12	3,01
7	-6,45	3,68
8	-5,71	4,42
9	-5,13	5,00
10	-4,31	5,82
11	-3,79	6,34
12	-3,45	6,68
13	-3,00	7,14
14	-2,14	7,99
15	-1,64	8,50
16	-1,14	9,00
17	-0,95	9,20
18	-0,75	9,40
19	-0,54	9,60
20	-0,35	9,80
21	-0,16	10,00
22	0,26	10,40
23	0,65	10,80
24	0,85	11,00

No	Vin Volt	Vout Volt
25	1,261	11,40
26	1,856	12,00
27	2,38	12,52
28	2,85	13,00
29	3,25	13,40
30	3,65	13,80
31	4,06	14,20
32	4,64	14,80
33	5,16	15,30
34	5,87	16,00
35	6,26	16,40
36	6,67	16,80
37	7,07	17,20
38	7,27	17,40
39	7,87	18,00
40	8,07	18,20
41	8,50	18,60
42	8,87	19,00
43	9,38	19,50
44	9,87	20,00
45	10,45	20,50
46	10,95	21,00
47	11,87	22,00

Çizelge 3.1. Şekil 3.6 daki devreden elde edilen V_{in} - V_{out} değerleri

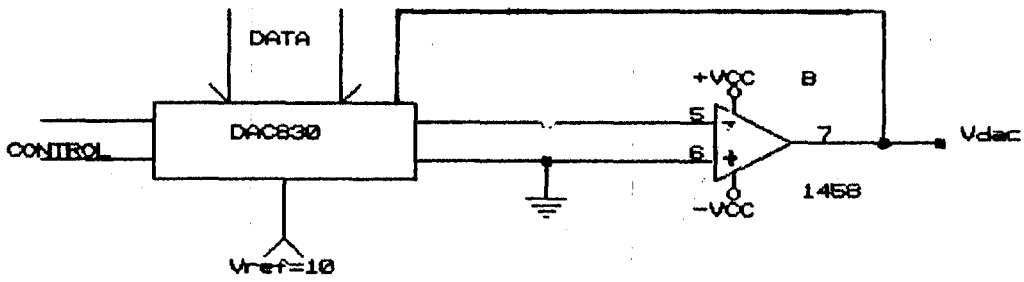


Şekil 3.7. Çizelge 3.1 deki değerlerle elde edilen V_{out}-V_{in} grafiği

Sistemde 8-bit'lik CMOS Digital/Analog Converter DAC830 kullanılmıştır. DAC830 referans girişine uygulanan ±10 V luk referans gerilimine ve kurulan devre yapısına bağlı olarak simetrik veya tek yönlü akım üretir. DAC830 hakkında geniş bilgi Ek.2'de verilmiştir. Sistemde uygulanan Şekil 3.8'deki devre yapısı ile DAC830 çıkışı 0 V - 10 V arası değişmektedir.

Türetilen (3.4) eşitliğine göre regülatör çıkışında 25 V elde etmek için V_{in} geriliminin 15 V olması, 0 V elde etmek için ise -10 V olması gerekir. Bunun için Şekil 3.8 deki devrede elde edilen -10 V luk gerilimin -10 V ile +15V arası değişmesi sağlanarak regülatör ayar bacağına uygulanması gerekir. Toplayıcı ve yükselteç görevini yerine

getiren Şekil 3.9 'daki devre bu amaçla tasarlanmıştır. Devrede gerilime çevrilmiş DAC830 çıkışı +5 V ile toplanmakta ve 3 ile çarpılmaktadır.



Şekil 3.8. DAC830

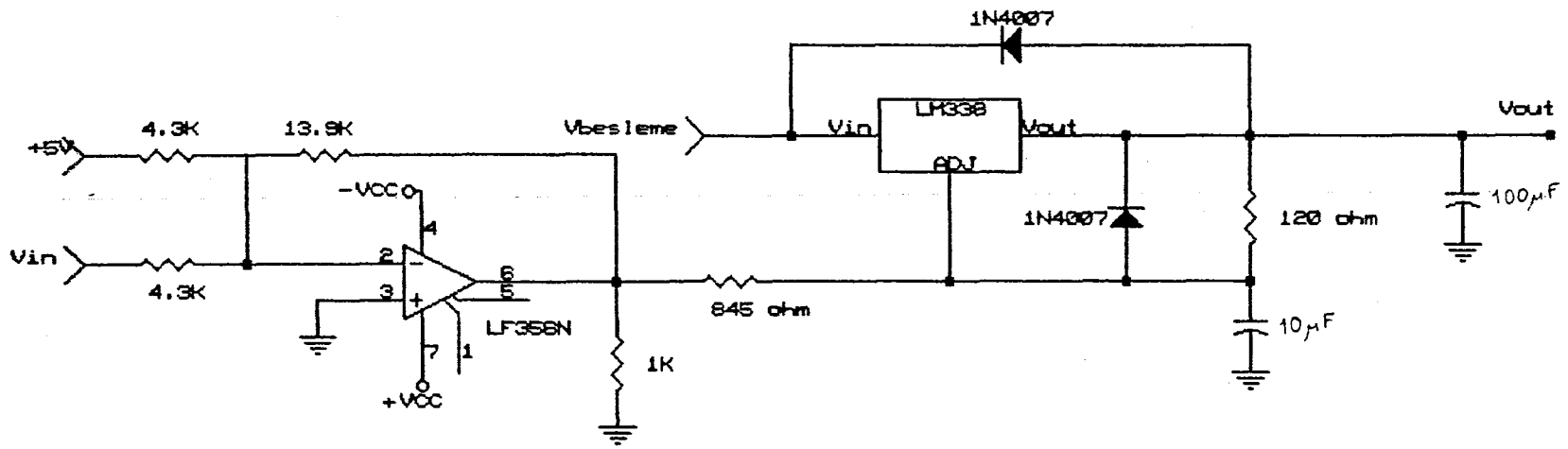
3.4. Mikroişlemci Kartı

Mikroişlemci kartı Şekil 3.10'da görüldüğü gibi mikroişlemci ve çevre birimlerinden oluşur.

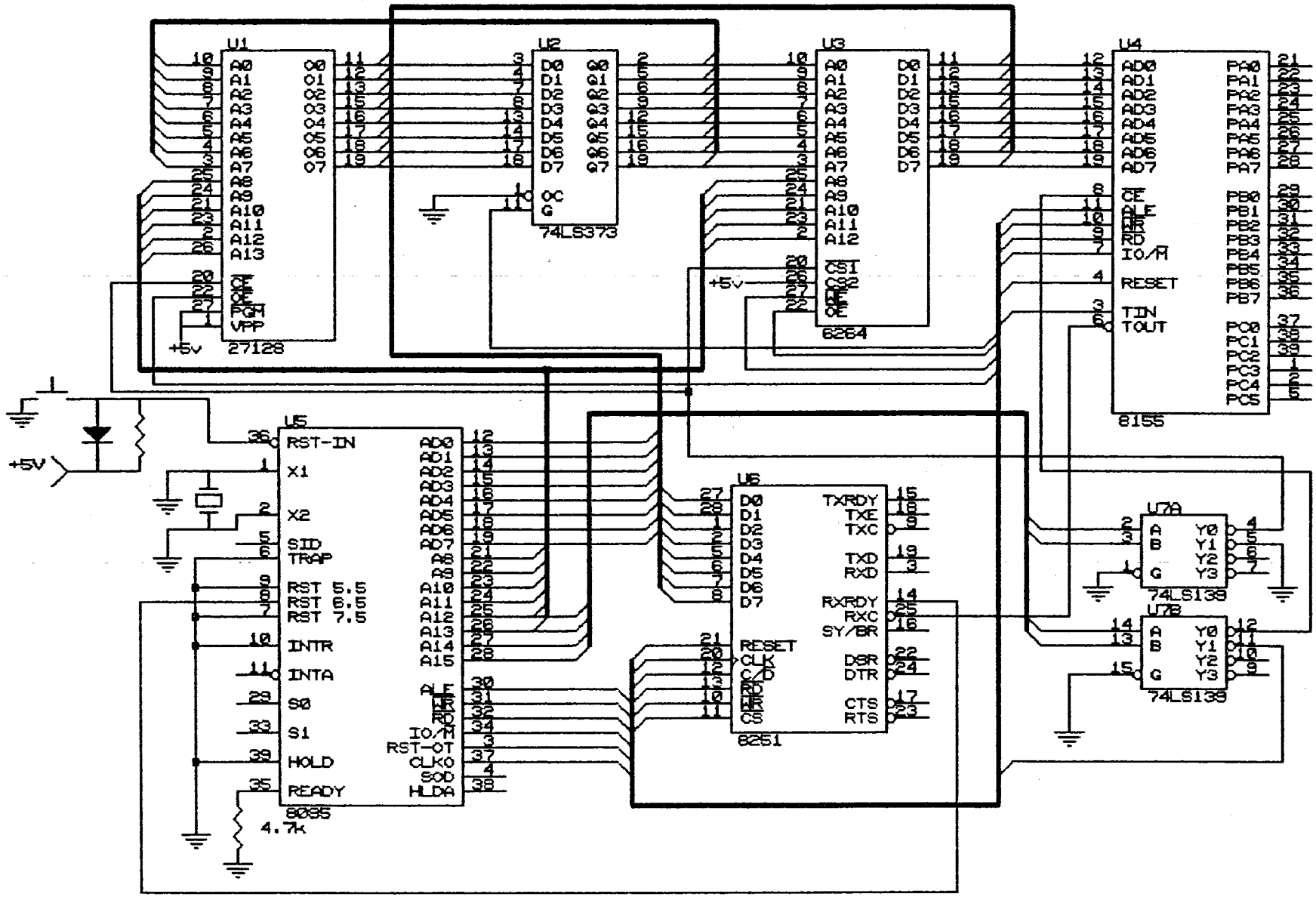
3.4.1. Mikroişlemci

Mikroişlemci olarak Intel firmasının 8-bitlik 8085A mikroişlemcisi kullanılmıştır. Bu mikroişlemci çoğullanmış veri hattı kullanır. 16-bit'lik adres hattının 8-biti ve 8-bit veri hattı aynı hattı kullanırlar. 8085A'da ilave olarak SIM ve RIM komutları vardır. Mikroişlemci kendi içinde saat üretecine sahip olup maksimum 3 MHz saat frekansı ile çalışabilmektedir.

8085A mikroişlemcisinde üç tür kesici (interrupt) vardır. Birincisi kurma (reset) kesicisidir. Bu kesici ilk anda adres sayıcının 0000H adresinden başlatılması için kullanılır. İkinci kesici türünde, biri maskelenemeyen dört tane kesici vardır. Bu kesicilerden biri geldiğinde mikroişlemci daha önceden belirlenmiş adresten itibaren çalışmaya başlar. RST 7.5, RST 6.5, RST 5.5 kesicileri yazılım ile engellenebilen, TRAP kesicisi ise yazılım ile engellenemeyen kesici girişidir. Üçüncü kesici türü ise INR kesicisidir. Bu kesici genel amaçlı olup yazılım ile engellenebilir.



Şekil 3.9. DAC830 Çıkışı toplayıcı ve regülatör ile bağlantısı



Şekil 3.10. Mikroişlemci kartı

8085A mikroişlemcisi ayrıca seri veri girişine ve çıkışına olanak sağlayan SID (Serial Input Data) ve SOD (Serial Output Data) bacaklarına sahiptir. Bu mikroişlemci, kendi ailesinden çevre elemanlarıyla yazılım ve donanım üstünlükleriyle birçok sistemde yaygın olarak kullanılmaktadır.

3.4.2. Giriş/çıkış birimi

Giriş/çıkış birimi olarak bir adet 8155 PIO (Parallel Input/Output) tümdevresi kullanılmıştır. 8155 PIO iki yönlü (giriş/çıkış) veri transferi için programlanabilen 2 adet 8-bitlik, 1 adet 6-bitlik giriş/çıkış portuna sahiptir. Ayrıca 8155 PIO, 256-byte'lık bir RAM ve programlanabilir 14-bitlik sayıcı/zamanlayıcı (counter / timer) içerir. Port ve sayıcı/zamanlayıcının kontrolu kumanda yazacına yazılan belirli şekildeki kontrol kelimeleri ile sağlanır.

3.4.3. Bellek

Sistemde yazılan programların, sabitlerin ve tabloların saklanması için EPROM kullanılmıştır. EPROM 16 KB lık olup 0000H - 3FFFH adresleri arasında kullanılmaktadır.

Sistemin geçici değişkenlerini ve kullanıcının girdiği anlık bilgileri saklamak için 8 KB lık RAM kullanılmıştır. RAM, 4000H - 4FFFH adreslerini kullanmaktadır.

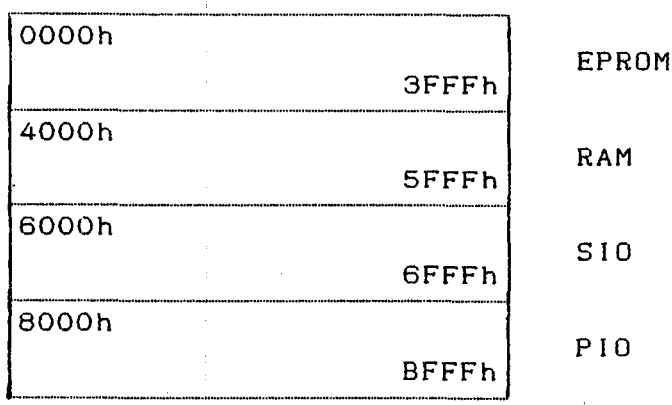
3.4.4. Seri giriş/çıkış (SIO) birimi

Sistemin seri giriş/çıkış birimi bulunan herhangi bir bilgisayar ile haberleşebilmesi için 8251 giriş/çıkış birimi kullanılmıştır. 8251 için gerekli olan saat, 8155 PIO zamanlayıcısından sağlanır. 8251 tümdevresi 8085 mikroişlemcisi ile doğrudan uyumlu senkron/asenkron alıcı/verici kombinasyonundan oluşmaktadır. Asenkron çalışmada bu eleman bilgi alışverişini 19200 baud-rate'e kadar yapabilmektedir. Senkron çalışmada 8251, otomatik olarak bir veya iki senkron karakterini veri aralarına yerleştirir. Bu çalışma modunda

bilgi alışverişi 64000 baud-rate hıza kadar yapılabilir.

3.4.5. Yardımcı tümdevreler

Mikroişlemci kartında bir adet 74139 adres çözücü kullanılmıştır. Adres çözücü, belirli bir bellek haritasına uygun olarak EPROM, RAM, 8155 PIO, 8251 SIO çevre birimlerinin seçilmesini sağlar (Şekil 3.11.).



Şekil 3.11. Bellek Haritası

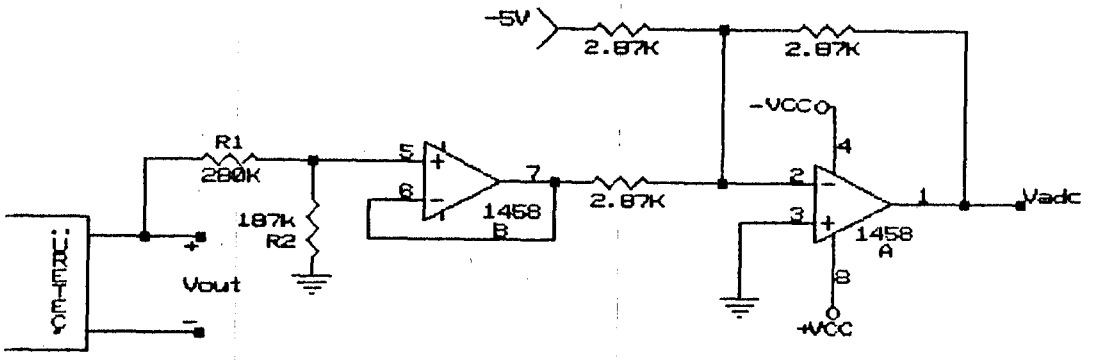
3.5. Geri Döngü Kontrol Sistemi

Üreteç çıkışı istenen bir gerilim değerine mikroişlemci aracılığıyla ayarlandıktan sonra çıkışta olması gereken gerilim değeri ve izin verilen maksimum akım değeri gene mikroişlemci tarafından üretecin çalışması süresince kontrol edilir.

3.5.1. Çıkış gerilimi kontrolu

Üreteç çıkış gerilimi mikroişlemci tarafından sürekli olarak kontrol edilerek giriş gerilimi ve yük değişimlerine karşı istenen sınırlar içerisinde kalması sağlanır. Böylelikle ikinci bir regülasyon sağlanmış olur.

Gerilim kontrol geri döngüsü bir gerilim bölücü, işlemsel kuvvetlendiricilerden oluşan uygunlaştırıcı ve analog/digital çevirici (ADC)'den oluşur (Şekil 3.12.).



Şekil 3.12. Çıkış gerilimi ölçümü

Devrede, önce çıkış gerilimi R_1 ve R_2 dirençleriyle 2,4'e bölünmekte; böylelikle 0 - 24 V arası değişen çıkış gerilimi 0 - 10 V a düşürülmektedir. R_1 ve R_2 dirençleri çıkışı etkilememek için yüksek değerli dirençlerden seçilmiştir. Gerilim bölücü çıkışında elde edilen 0 - 10 V luk gerilim -5 V ile toplanarak ADC girişine uygun (-5 V) - (+5 V) aralığında bir gerilime çevrilir (V_{ADC}). V_{ADC} gerilimi 8-bit'lik analog/digital çevirici ADC800 ün analog girişine uygulanır. 8-bit'lik nümerik bilgiye çevirilen V_{ADC} gerilim seviyesi mikroişlemci tarafından okunarak kullanılır. 24 V luk gerilim seviyesi FFH nümerik değerine 0 V luk gerilim seviyesi de 00H nümerik değerine karşılık gelir.

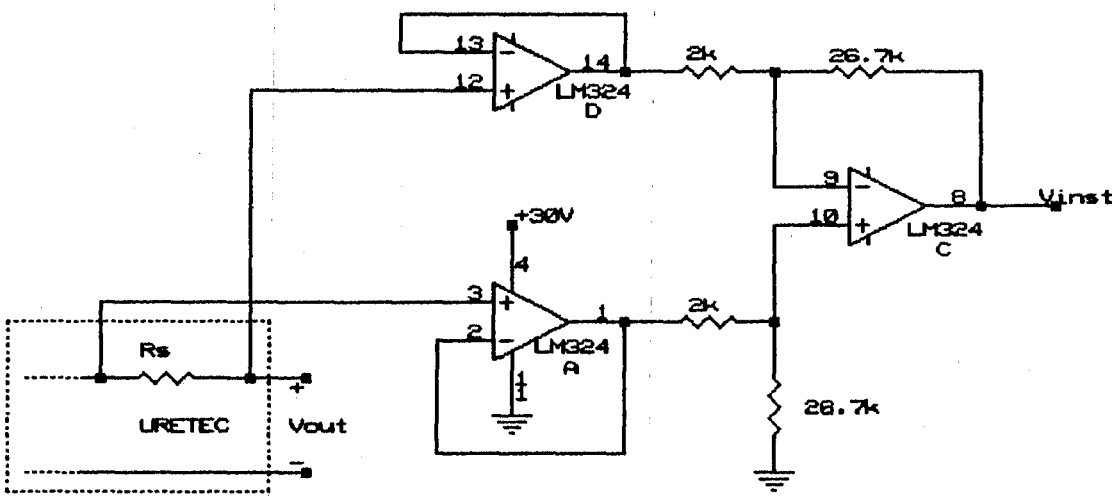
ADC800, 50 KHz ile 800 KHz frekans aralığında çevirme yapabilir. ADC800 için gerekli saat sinyali 8155 PIO zamanlayıcısı tarafından sağlanır. Çevirici "Start Conversion" girişine uygulanan başlama komutuyla çevirme işlemine başlar ve çevirme işlemi bitiminde "EOC" (End Of Conversion) çıkışı "logik 1" 'e çekilir. Böylelikle EOC çıkışı gözlenerek çevirme işlemi sonunda 8-bit'lik nümerik bilgi "OE" (Output Enable) girişine "logik 1" uygulandıktan sonra okunabilir. ADC800 hakkında geniş bilgi Ek.3'te verilmiştir.

3.5.2. Çıkış akımı kontrolu

Kullanıcı tarafından verilen maksimum çıkış akımı (bu değer 5 A den küçük olmalıdır), hafızada saklanarak üre-

teç çıkışındaki akım değeri ile sürekli olarak karşılaştırılır. Eğer çıkışta ölçülen akım değerinin hafızadaki değerden büyük olduğu gözlenirse mikroişlemci üreteci yükten ayırır ve yüksek akım çekildiğini belirten mesaj verir.

Akım kontrol geri döngüsü, üreteç çıkışına seri bağlı bir direnç ve bu direnç uçları arasındaki gerilim farkını yükselten bir instrumantasyon yükseltecinden oluşur. (Şekil 3.13.).

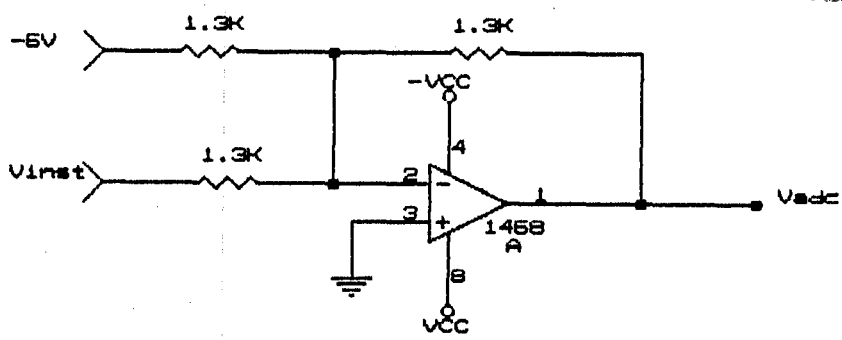


Şekil 3.13. Çıkış akımı ölçümü

üreteç çıkışına seri bağlı R_S direnci akımı gerilime çevirir. Üzerindeki gerilim düşümünü azaltmak için bu direncin değerinin çok küçük seçilmesi ve yeterli güçte olması gerekir. Sistemde kullanılan R_S direnci 0,15 Ohm 5 W lıktır. Dirençten maksimum 5,77 A akım geçebilir.

R_S direncinden sonra yer alan instrumantasyon yükselteci yüksek giriş empedansına sahip bir fark yükseltecidir. Instrumantasyon yükselteci, üç adet yüksek gerilimde (32 V) çalışabilen işlemsel kuvvetlendiriciden oluşur. Yükselteç çok yüksek giriş empedansına sahip olduğundan R_S direnci uçlarından akım çekmez fakat direnç uçları arasındaki gerilim farkını yükseltir. Yükselteç kazancı olarak 13,3 seçilmiştir. R_S direnci üzerindeki en yüksek gerilim düşümü üreteç uçlarından en yüksek akım geçtiğinde oluşur. Bu da

0,75 V tur. Bu gerilim 13,3 kazançlı instrumantasyon yükselteci ile 10 V a yükseltilmektedir. 0-10 V arası değişen V_{inst} gerilimi analog/digital çeviriciye verilmeden önce Şekil 3.14'teki devre ile (-5 V) - (+5 V) arası gerilime çevrilmektedir. Bu devre 1 kazançlı bir toplayıcıdır.



Şekil 3.14. Toplayıcı devresi

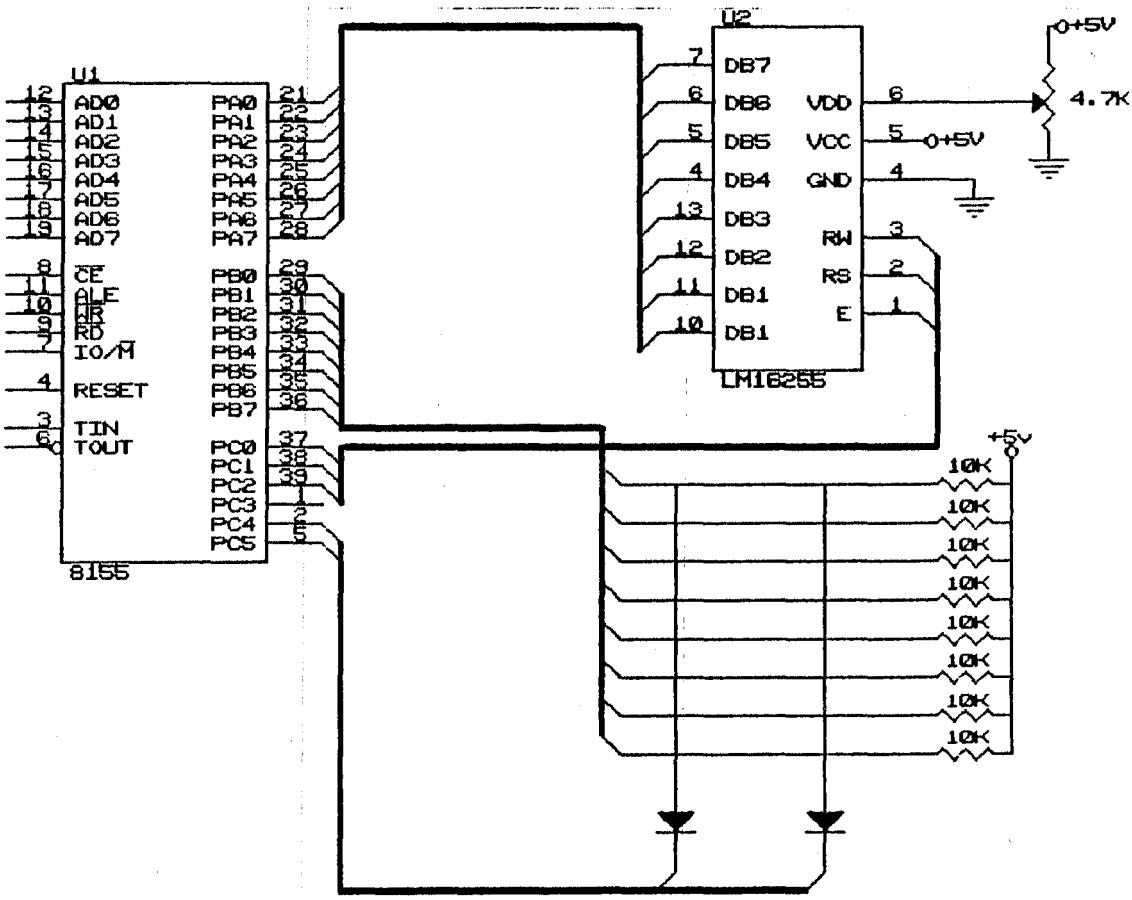
Çıkış akımı ve gerilimi bir tek ADC üzerinden okunmaktadır. Bunun için ADC800 girişine 4051 multiplexer yerleştirilmiştir. Böylelikle mikroişlemci multiplexer seçme girişlerini değiştirerek akım veya gerilimi ADC'den okur.

3.6. Tuş Takımı ve Gösterge

Programlanabilir gerilim üretecinde 16 adet tuş vardır. Kullanıcı her türlü veri girişini ve programlamayı bu 16 tuş ile yapar. Tuş takımında 0'dan 9'a kadar rakamlar, RUN, RESET, V_{out}, I_{out}, V_{tol} ve nokta tuşları vardır. Tuş takımı 8055 PIO'nun 8-bitlik B portuna ve C portunun 2-bitine bağlıdır. Mikroişlemci, tuş takımından bilgi beklerken sürekli olarak tuşları tarar. Herhangi bir tuşa basıldığını tesbit ederse bu tuşla ilgili gerekli işlemleri yapar.

Sistemde kullanıcı ile iletişim sağlamak amacıyla LCD gösterge (LM16255) kullanılmıştır. LM16255 göstergesi iki satırlıktır ve herbir satıra 16 karakter yazılabilir. Göstergenin kendi belleği ve tarama devreleri olduğundan mikroişlemci sadece veri gönderirken gösterge ile bağlantı kurar. LCD göstergenin veri hattı 8155 PIO A portuna; kont-

rol sinyalleri ise C portunun 3-bit'ine bağlıdır (Şekil 3.15.).



Şekil 3.15. Gösterge ve tuş takımının 8155 PIO ile bağlantısı

4.YAZILIM

Sistemde mikroişlemci olarak 8085 mikroişlemcisi kullanıldığından sistemi işleten programlar da 8085 assembler dilinde yazılmıştır.

Sistem programları modüler yapıda yazılmış olup her programa diğer bir programdan ulaşmak mümkündür. Sistem, açılış programı tarafından yönetilir. Yerine getirilecek fonksiyona göre bu program ilgili alt programları çağırır. Alt programlar gene küçük alt programlardan meydana gelir.

4.1 Akış Şemaları

Sisteme güç verildiğinde "açılış" programı çalışmaya başlar (Şekil 4.1.). Bu program önce sistem değişkenlerini başlangıç durumuna getirir ve 8155 PIO portları giriş veya çıkışa programlar. Bu işlemlerden sonra "Self Test" programı (Şekil 4.2.) çalıştırılarak güç kaynağı çıkışının istenen şekilde programlanıp programlanamadığı kontrol edilir. Eğer test başarıyla sonuçlanırsa kullanıcının bir fonksiyon tuşuna basması beklenir.

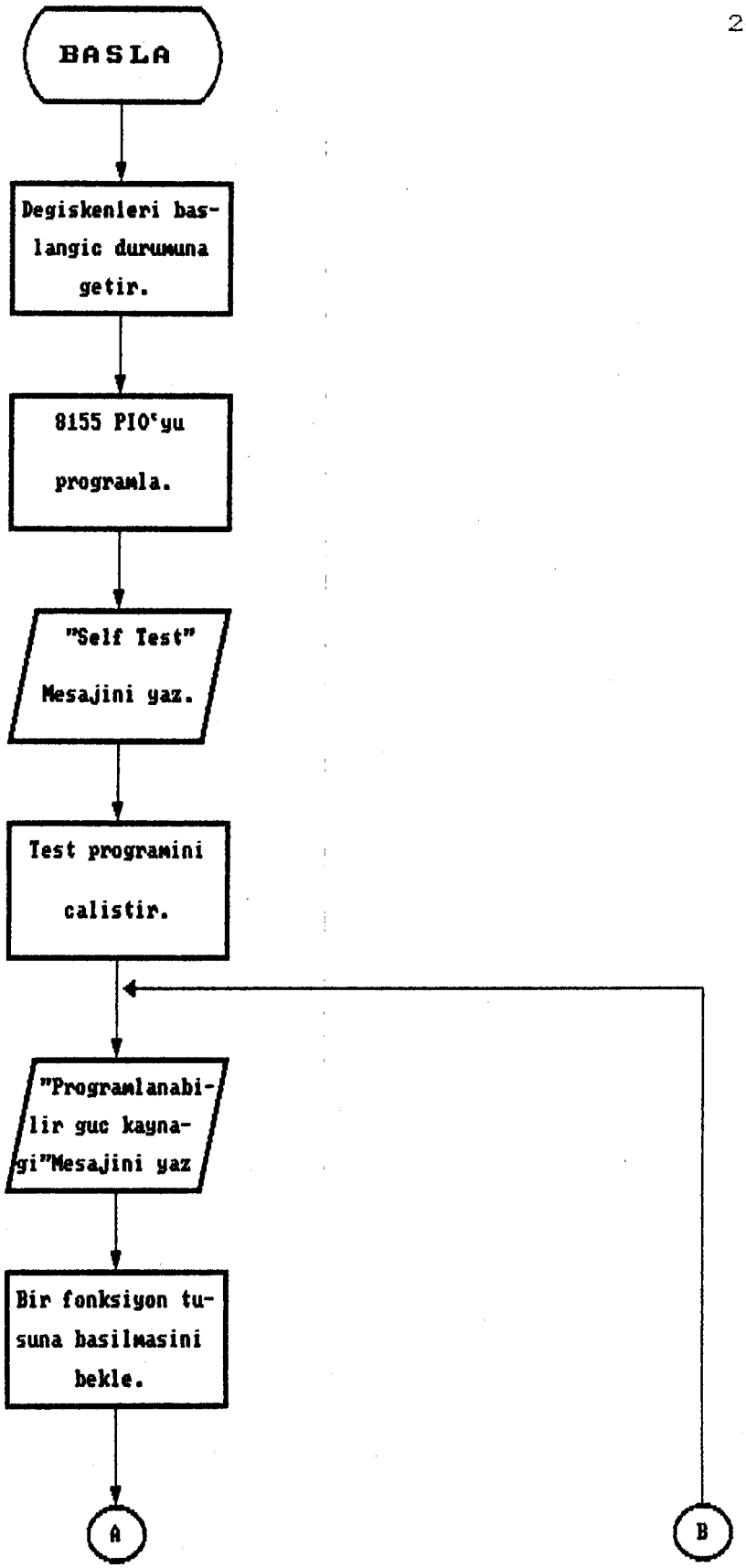
Eğer kullanıcı V_{out} tuşuna basarsa güç kaynağı çıkışının olması istenen voltaj değeri volt cinsinden tuş takımı aracılığıyla girilir ve açılış programına geri dönülür. Bu işlemler "Get V_{out}" (Şekil 4.3.), "Get" (Şekil 4.6.) programları tarafından yapılır.

Aynı şekilde kullanıcı ilgili tuşlara basarak V_{tol},çıkış voltajı toleransı, I_{max}, izin verilen maksimum çıkış akımı değerlerini sisteme verir. Bu işlemler "Get V_{tol}" (Şekil 4.4.), "Get I_{max}" (Şekil 4.5.), "Get" (Şekil 4.6.) programları tarafından yapılır.

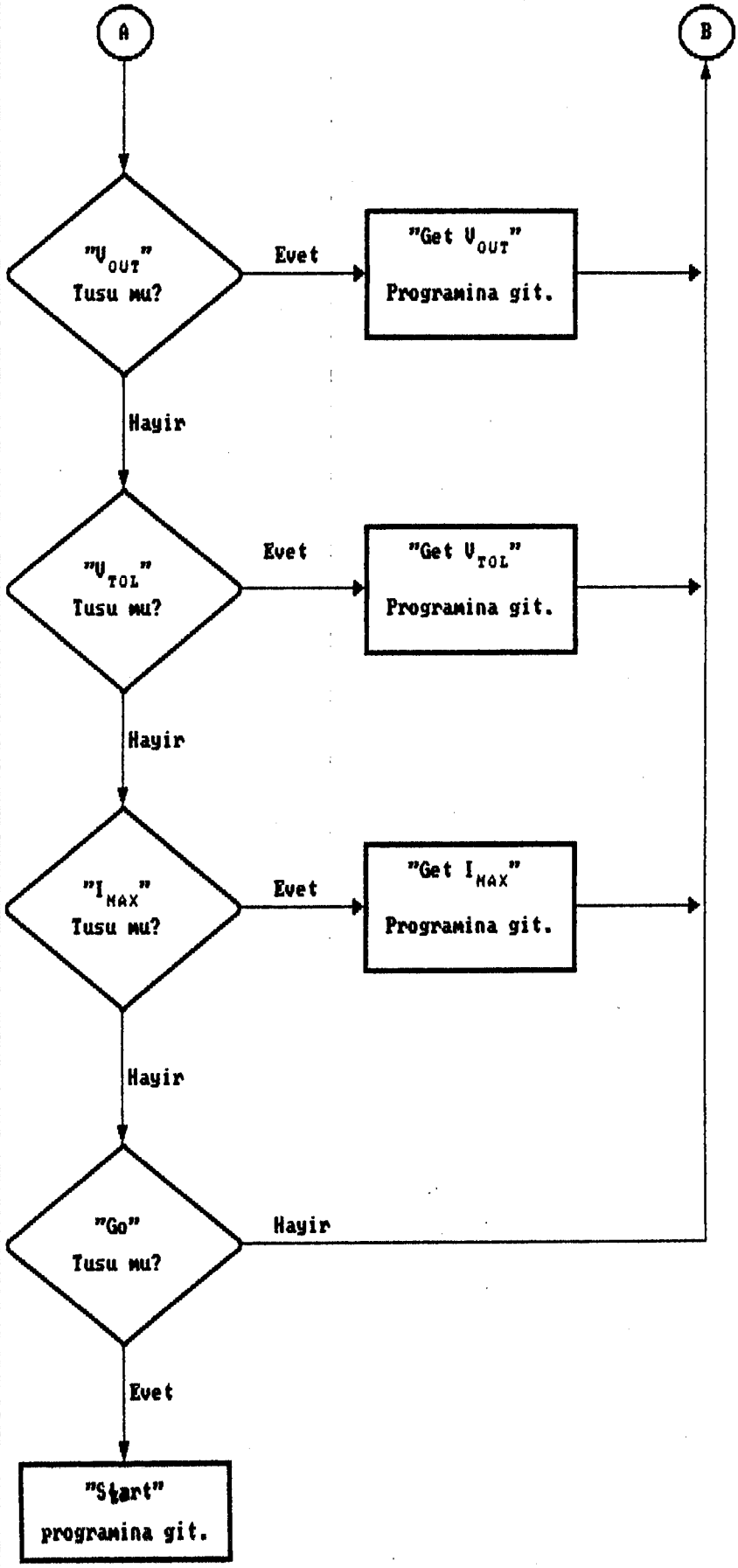
Kullanıcı güç kaynağı çıkışı ile ilgili bütün değerleri girdikten sonra "Go" tuşuna basarak güç kaynağı çıkışının girilen değerlere programlanmasını sağlar. Bundan sonra çıkış, mikroişlemci tarafından izlenerek kaynağın istenen limitlerde kalıp kalmadığı kontrol edilir. Bu

işlemler "Start" programı tarafından (Şekil 4.9.) gerçekleştirilir.

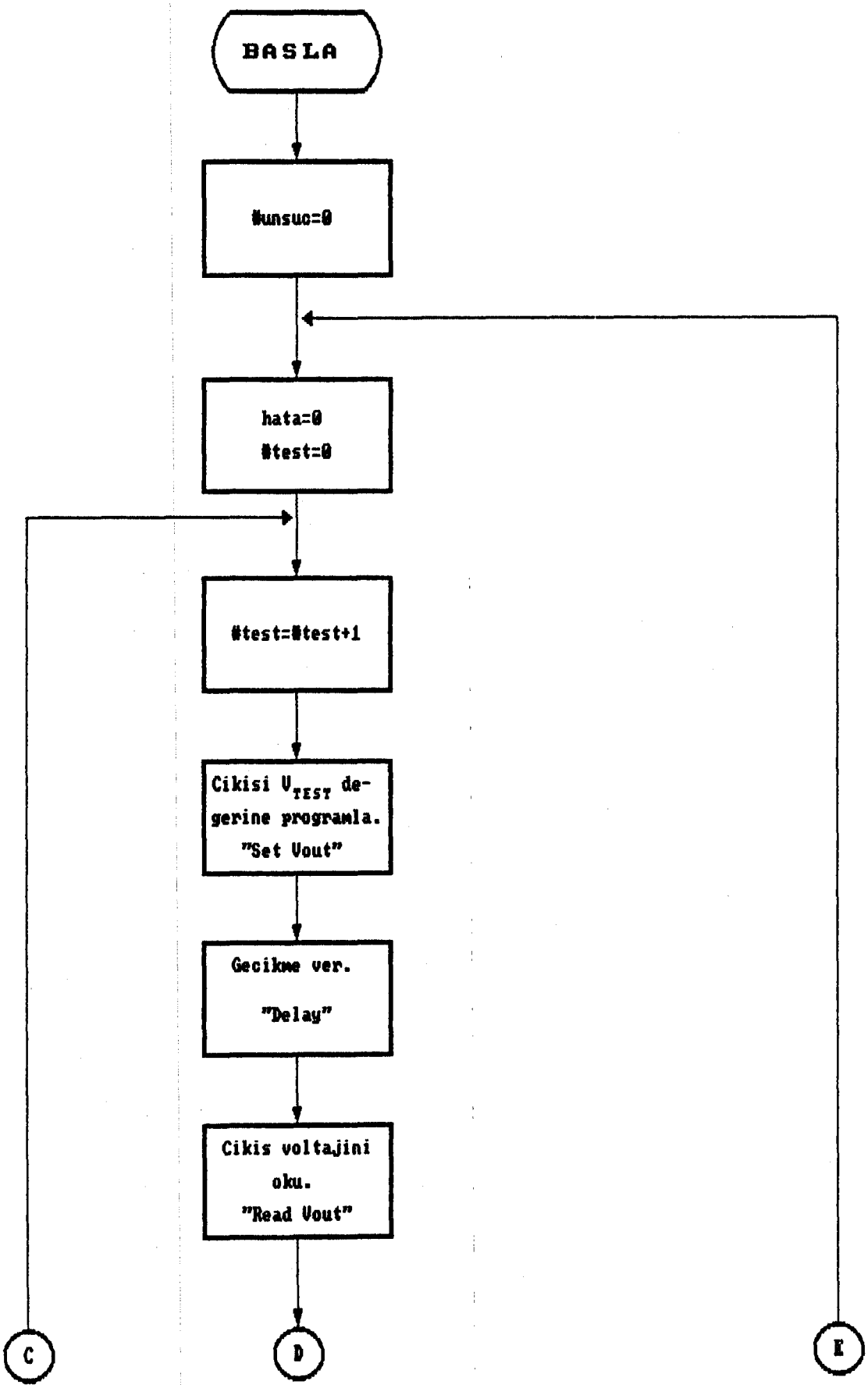
Sistem programları Ek 4. 'te verilmiştir.



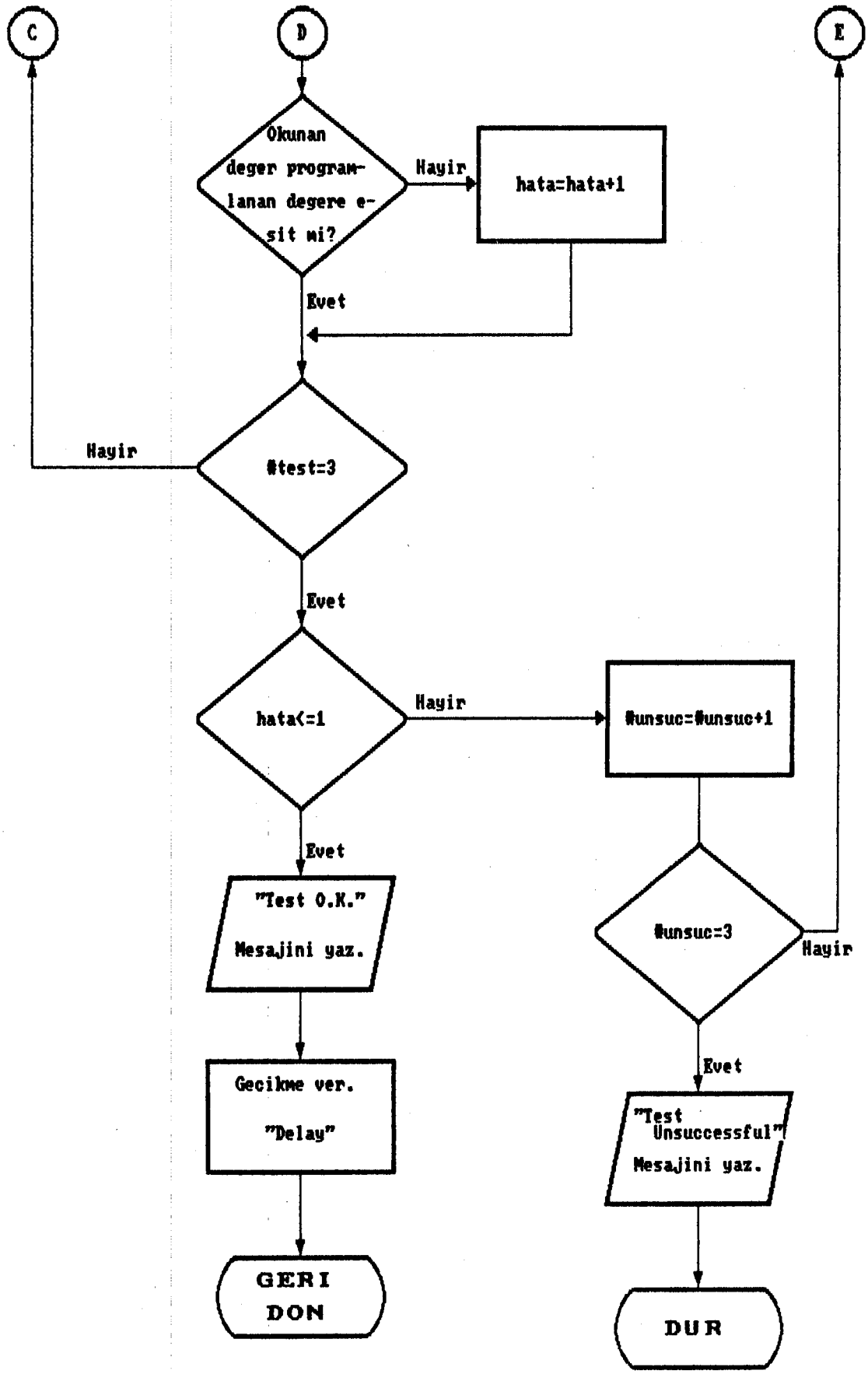
Şekil 4.1. Açılış programı akış şeması



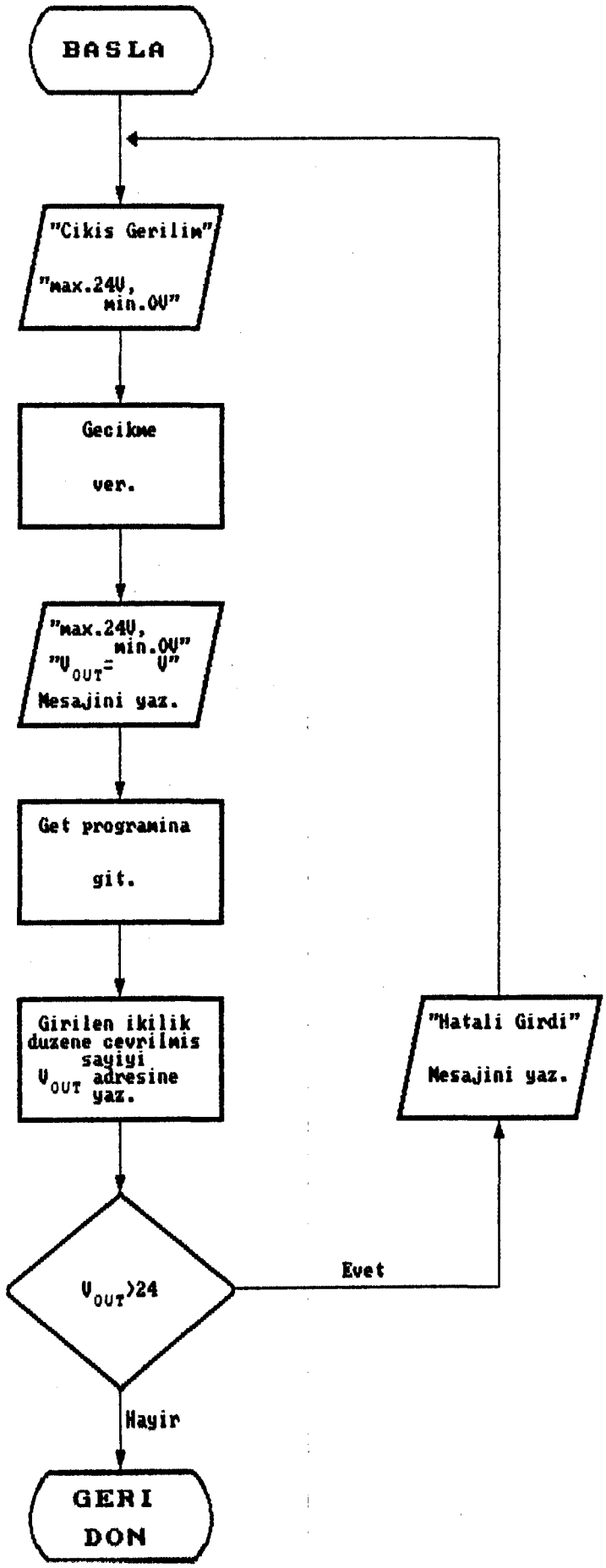
Şekil 4.1. Açılış programı akış şeması (devam)



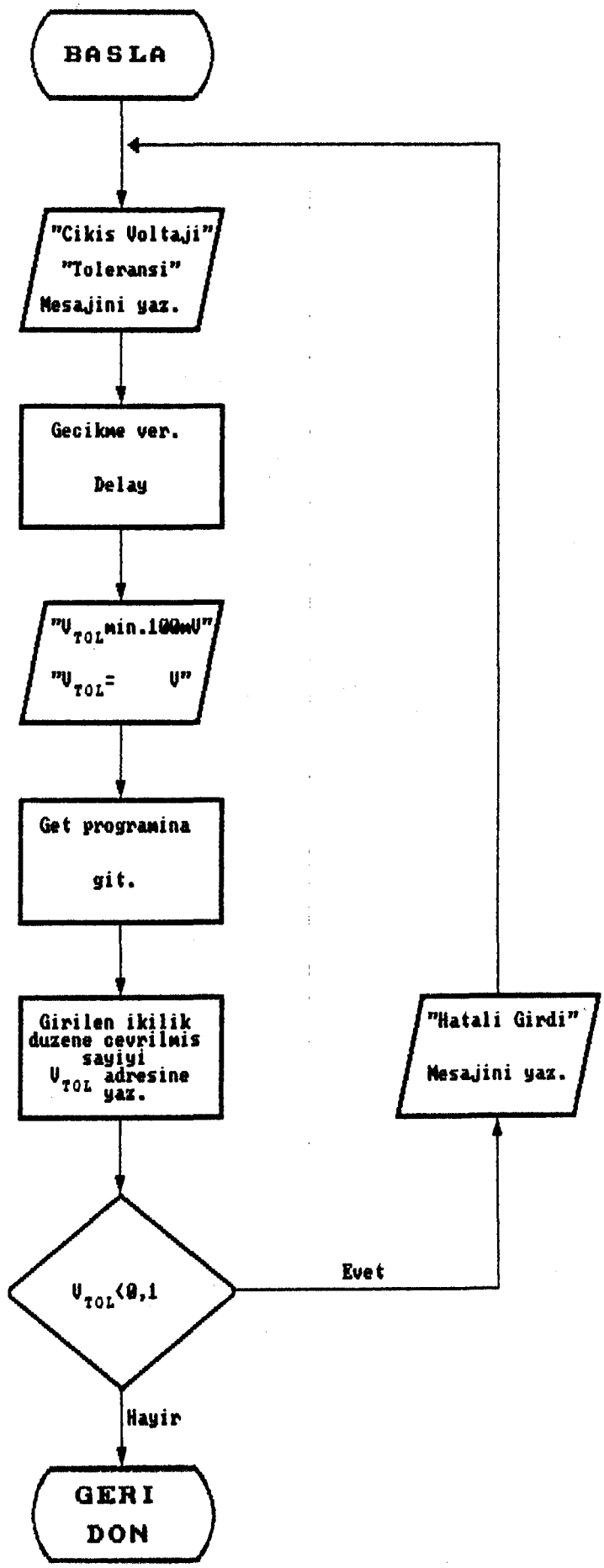
Şekil 4.2. Self test programı akış şeması



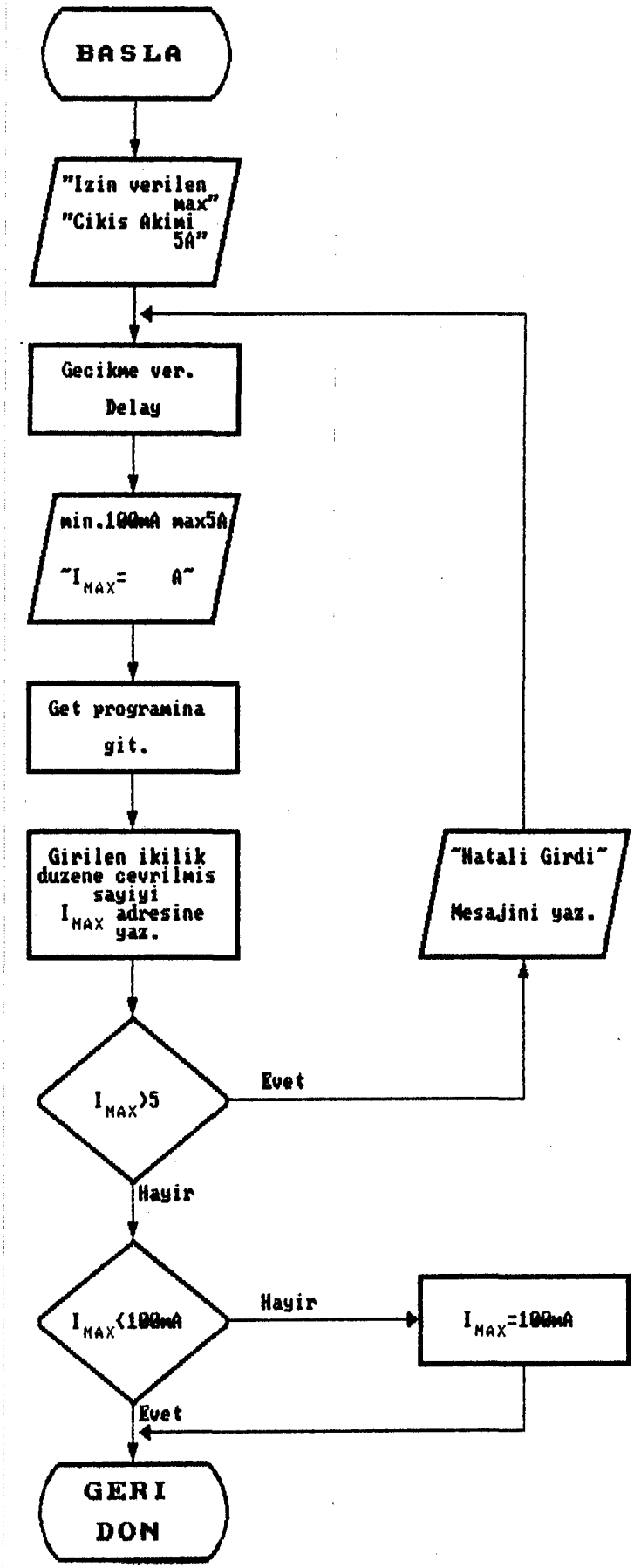
Şekil 4.2. Self test programı akış şeması (devam)



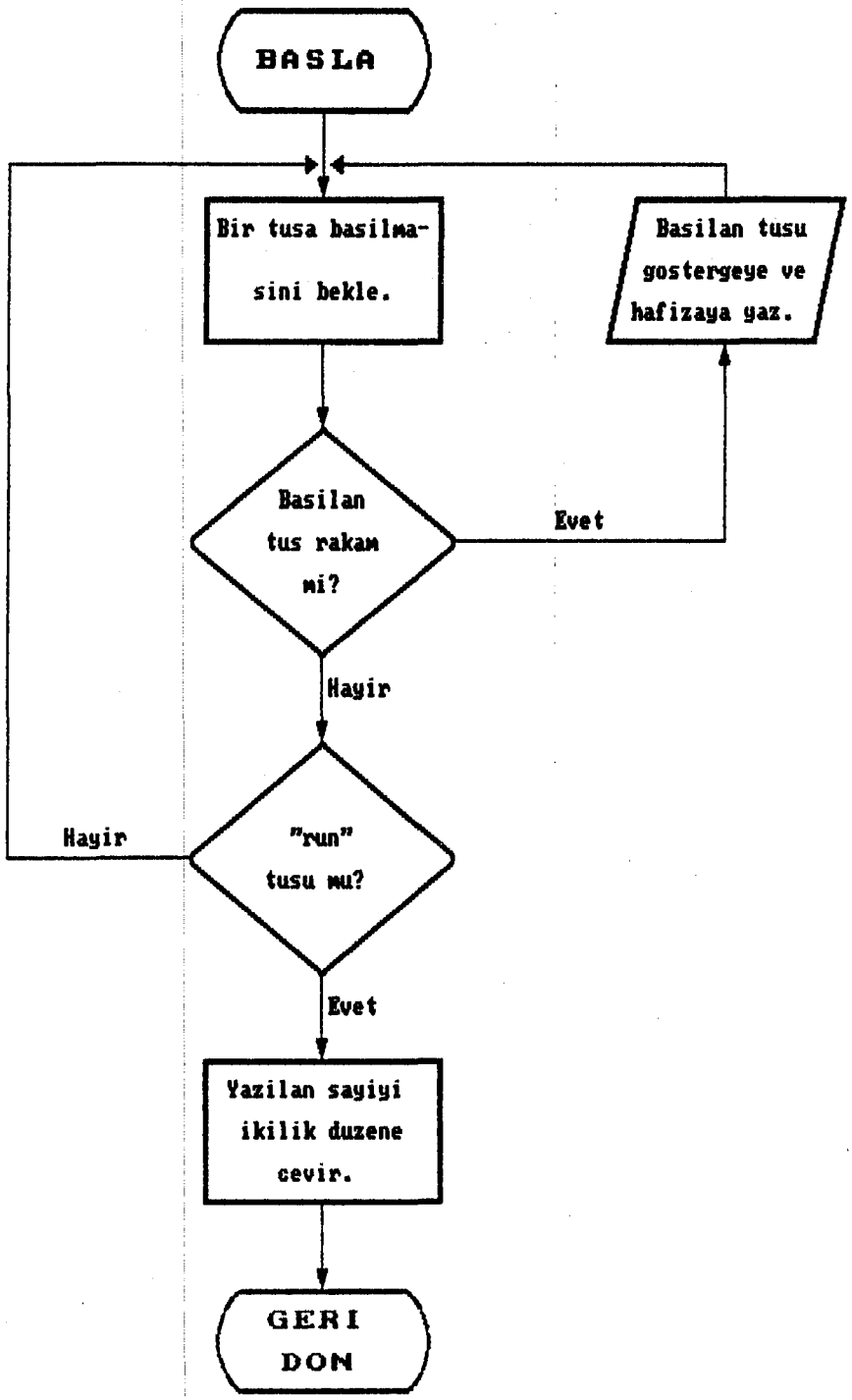
Şekil 4.3. Get V_{out} programı akış şeması



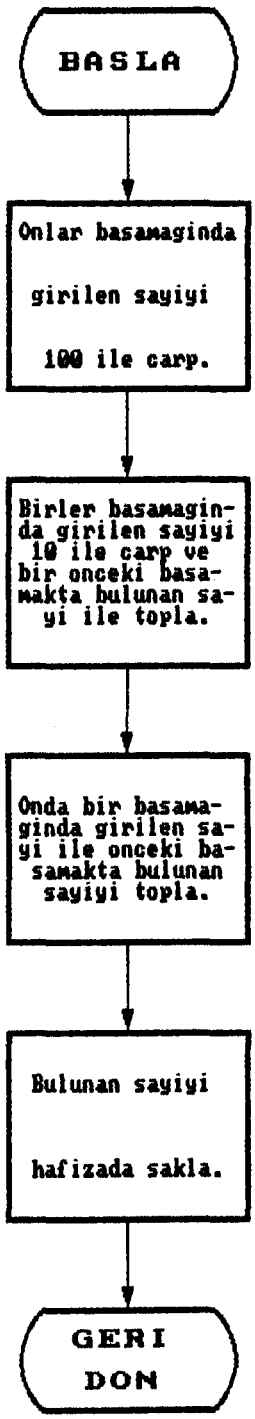
Sekil 4.4. Get V_{tol} programı akış şeması



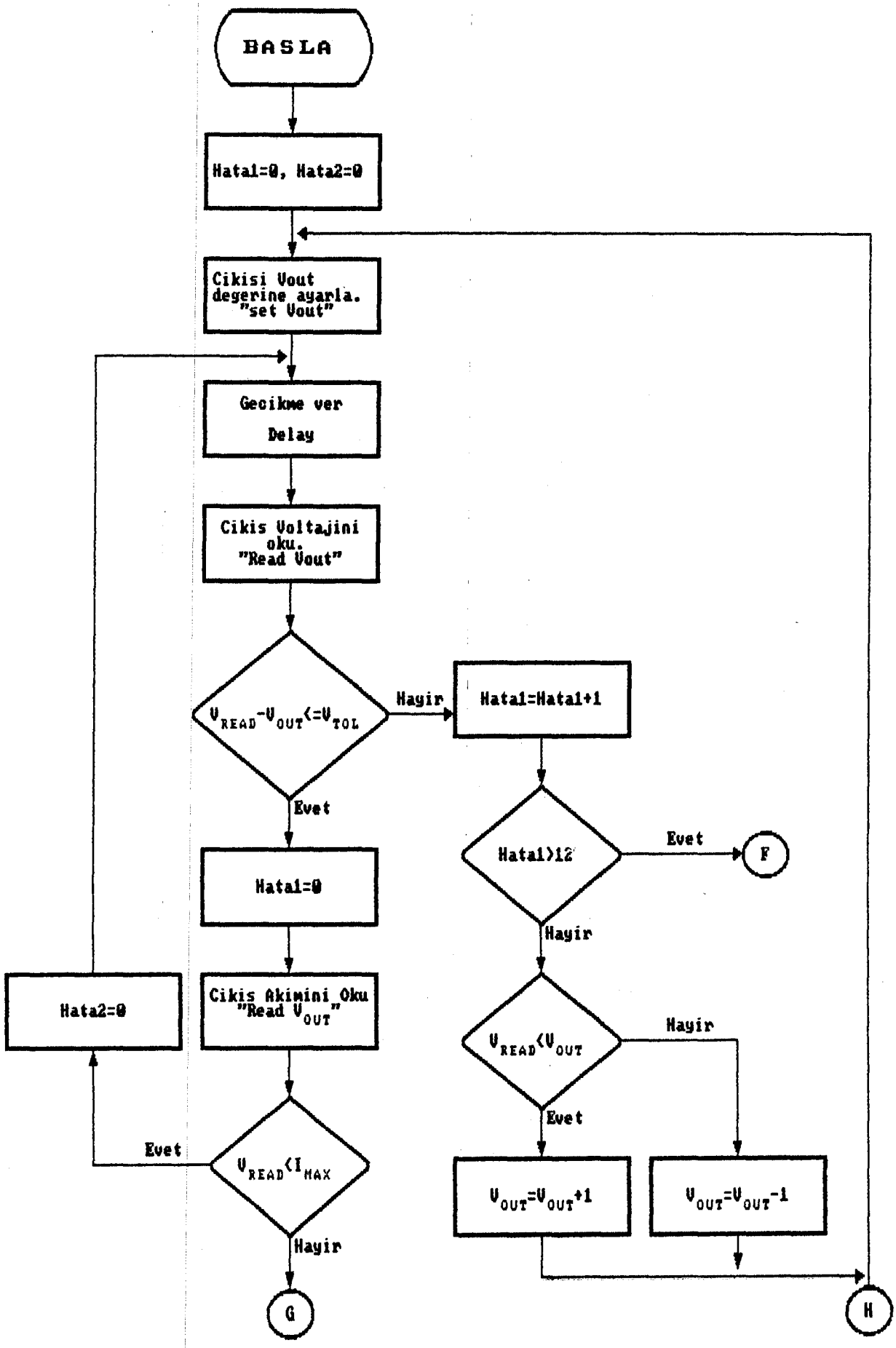
Şekil 4.5. Get I_{max} programı akış şeması



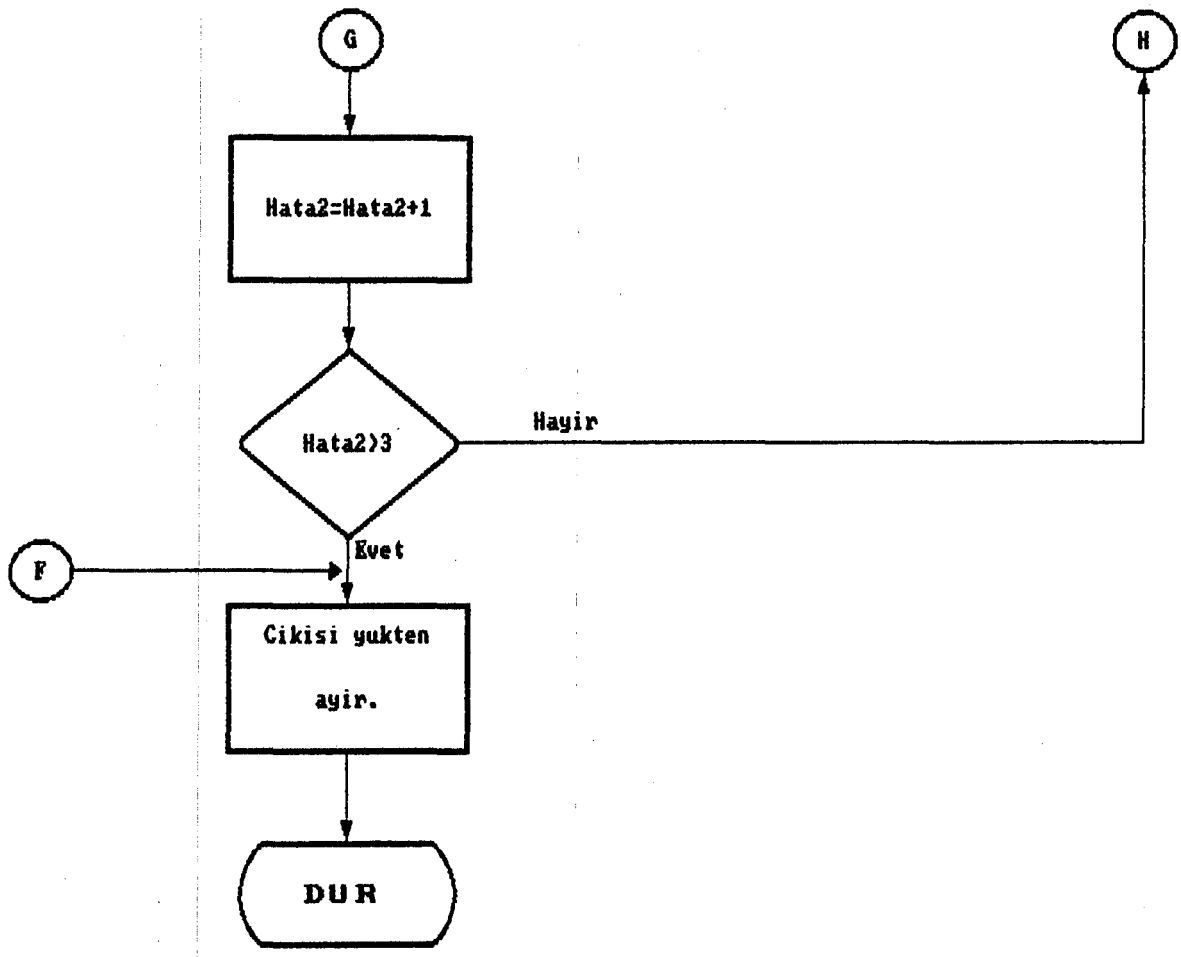
Şekil 4.6. Get programı akış şeması



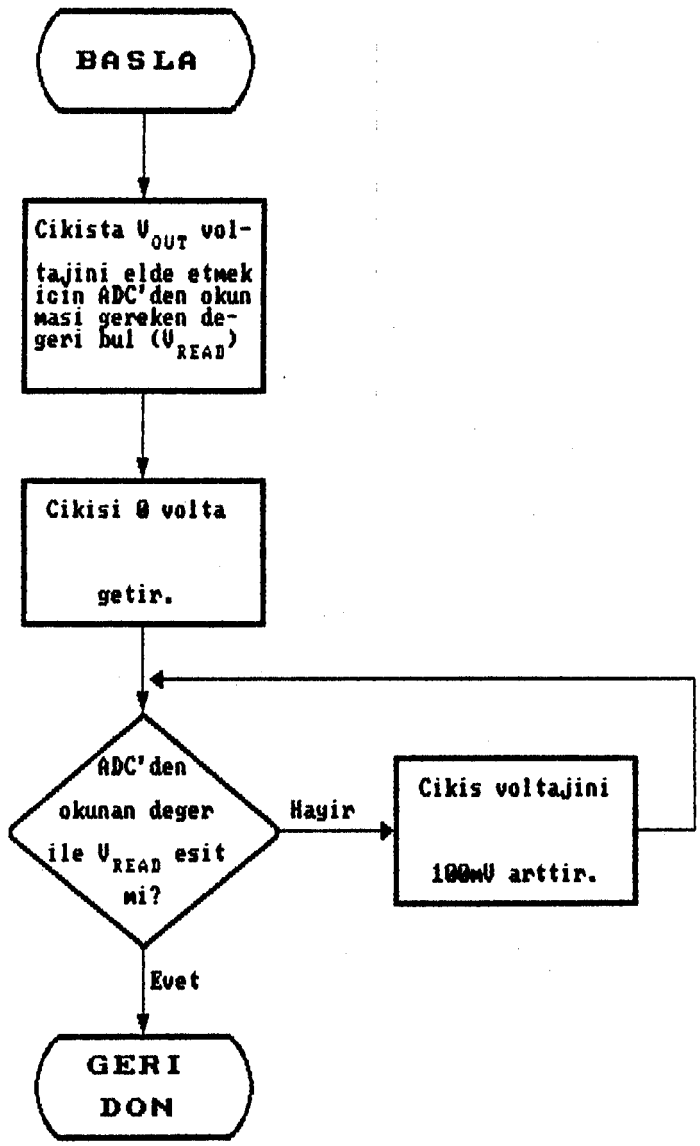
Şekil 4.7. DecBin programı akış şeması



Sekil 4.8. Start programı akış şeması



Sekil 4.8. Start programı akış şeması (devam)



Şekil 4.9. Set V_{out} programı akış şeması

5. SONUÇLAR

Bu çalışmada bir programlanabilir güç kaynağı gerçekleştirilmiştir. Cihaz bu haliyle çeşitli çalışmalarda güç kaynağı olarak kullanılabileceği gibi elektronik kartların test işlemlerinde de kullanılabilir. Programlanabilir güç kaynağı 0 V - 24 V arası 100 mV aralıklarla ±100 mV hassasiyette programlanabilmektedir. Çıkış katında yer alan LM338 regülatörünün teknik özelliklerinden dolayı cihaz çıkışından maksimum 5 A akım çekilebilir. Çıkıştan elde edilebilecek akım miktarı regülatör giriş ve çıkışı arasındaki gerilim farkına bağlıdır (bakınız Ek 1). Bu yüzden düşük gerilimlerde 5 A e kadar akım çekebilmek için LM338 regülatörü girişine uygulanan gerilim seviyesi bir röle ile değiştirilmektedir. Bu tez çalışmasında çıkış voltajı 0 V - 24 V arasında olacak şekilde tesarlanmıştır. Tasarımda aynı mantık ve LM338 regülatörü kullanılarak çıkış voltajı daha yüksek seviyelere çıkartılabilir. Bu işlem LM338 'in yüzen tipte (yani yalnızca giriş ve çıkış arasındaki gerilim farkına göre çalışan) bir regülatör olmasından yararlanılarak gerçekleştirilebilir.

Aynı anda birden fazla farklı gerilimlere gereksinim duyulan durumlarda çıkış katı ve kontrol devreleri sayısı artırılıp tek mikroişlemci sistemi ile çok çıkışlı programlanabilir güç kaynağı elde edilebilir.

100 mV tan daha hassas programlama istenen durumlarda ise çıkış voltajı aralığı düşürülmeli veya daha hassas digital/analog çevirici kullanılmalıdır. Ayrıca geri döngü kontrol sisteminde kullanılan analog/digital çevirici ve onun referans girişleri çok daha hassas olmalıdır.

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Stöhr, E., 1983, Programmable power supply, Elektor, October 1983, 49-50.

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National Semiconductor

Voltage Regulators

LM138/LM238/LM338
5 Amp Adjustable Power Regulators

General Description

The LM138/LM238/LM338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation — comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

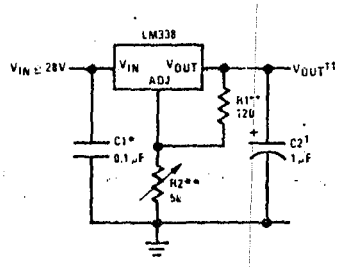
The LM138/LM238/LM338 are packaged in standard steel TO-3 transistor packages. The LM138 is rated for operation from −55°C to +150°C, the LM238 from −25°C to +150°C and the LM338 from 0°C to +125°C.

Features

- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- **100% electrical burn-in in thermal limit**
- Standard 3-lead transistor package

Typical Applications

1.2V–25V Adjustable Regulator



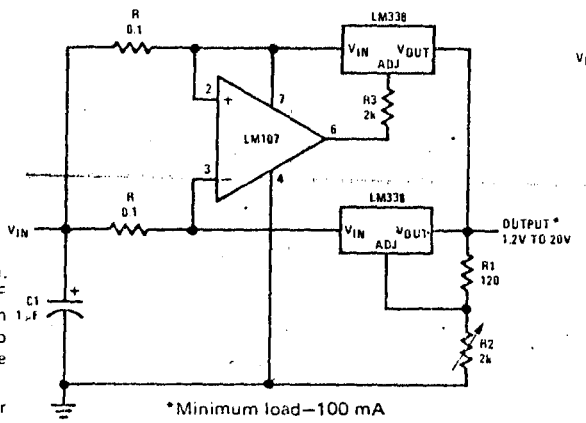
†Optional—improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is far from filter capacitors.

$$^{\dagger\dagger}V_{OUT} = 1.25V \cdot \left(1 + \frac{R2}{R1}\right)$$

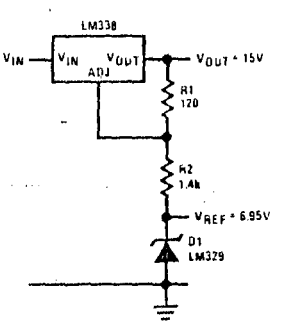
**R1 = 240Ω for LM138 and LM238
R1, R2 as an assembly can be ordered from Bourns:
MIL part no. 7105A-AT2-502
COMM part no. 7105A-AT7-502

10A Regulator



*Minimum load—100 mA

Regulator and Voltage Reference



Absolute Maximum Ratings

Power Dissipation	Internally limited
Input-Output Voltage Differential	35V
Operating Junction Temperature Range	
LM138	−55°C to +150°C
LM238	−25°C to +150°C
LM338	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit — **All Devices 100%**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM138-LM238			LM338			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \le V_{IN} - V_{OUT} \le 35V$, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	$T_A = 25°C$, $10mA \le I_{OUT} \le 5A$							
	$V_{OUT} \le 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \ge 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	Pulse = 20 ms		0.002	0.01		0.002	0.02	%/W
Adjustment Pin Current			45	100		45	100	μA
Adjustment Pin Current Change	$10mA \le I_L \le 5A$		0.2	5		0.2	5	μA
	$3V \le (V_{IN} - V_{OUT}) \le 35V$							
Reference Voltage	$3 \le (V_{IN} - V_{OUT}) \le 35V$, (Note 3)	1.19	1.24	1.29	1.19	1.24	1.29	V
	$10mA \le I_{OUT} \le 5A$, $P \le 50W$							
Line Regulation	$3V \le V_{IN} - V_{OUT} \le 35V$, (Note 2)		0.02	0.04		0.02	0.06	%/V
Load Regulation	$10mA \le I_{OUT} \le 5A$, (Note 2)							
	$V_{OUT} \le 5V$		20	30		20	50	mV
	$V_{OUT} \ge 5V$		0.3	0.6		0.3	1.0	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN} - V_{OUT} \le 10V$							
	DC	5.0	8		5.0	8		A
	0.5 ms Peak	7	12		7	12		A
	$V_{IN} - V_{OUT} = 30V$		1			1		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10 Hz \le f \le 10 kHz$		0.003			0.003		
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10 \mu F$	60	75		60	75		dB
Long Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package			1.0			1.0	°C/W

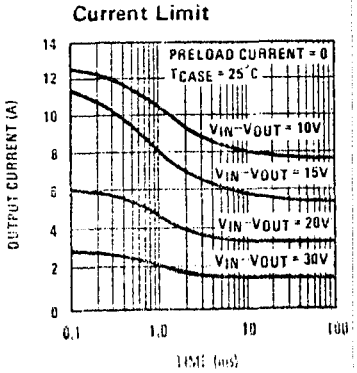
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM138, $-25°C \le T_j \le +150°C$ for the LM238 a $0°C \le T_j \le +125°C$ for the LM338, $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 2.5A$. Although power dissipation is internally limited, these specificatio are applicable for power dissipations up to 50W.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account se arately by thermal regulation.

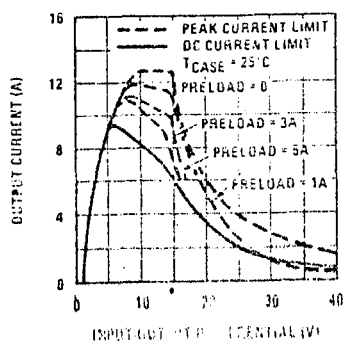
Note 3: Selected devices with tightened tolerance reference voltage available.

Typical Performance Characteristics

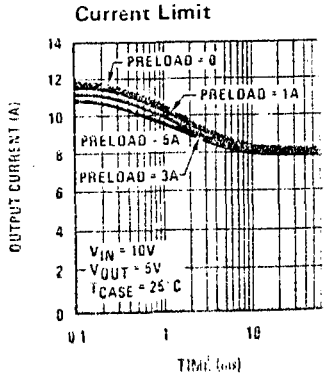
Current Limit



Current Limit

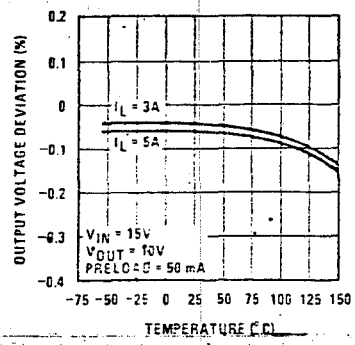


Current Limit

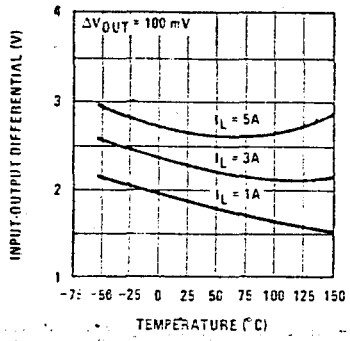


Typical Performance Characteristics (Continued)

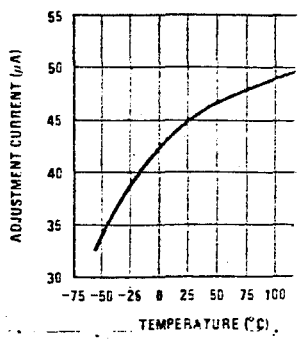
Load Regulation



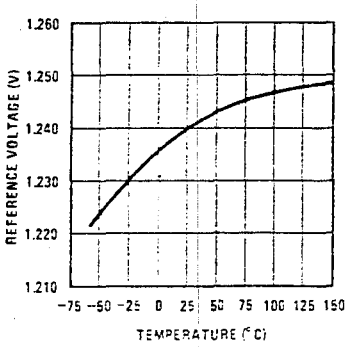
Dropout Voltage



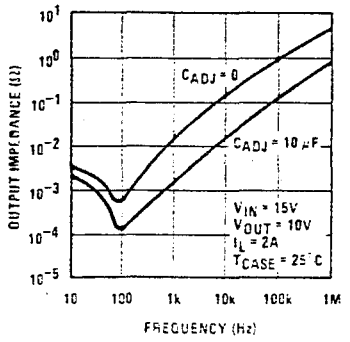
Adjustment Current



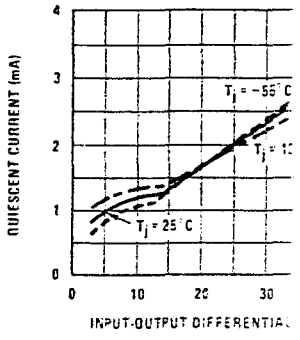
Temperature Stability



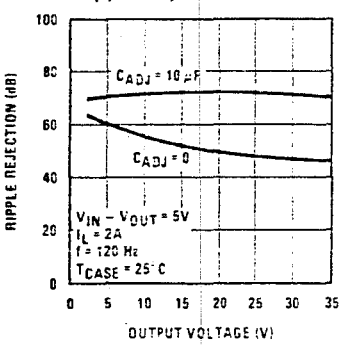
Output Impedance



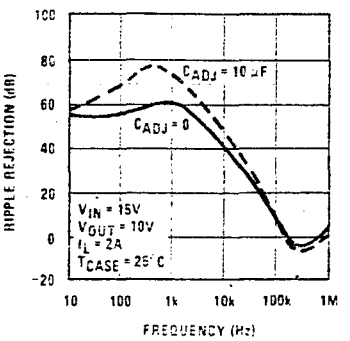
Minimum Operating Current



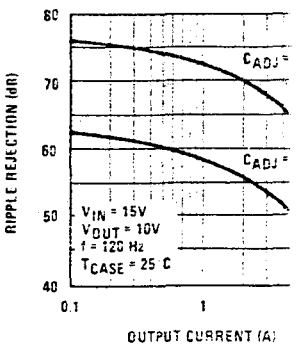
Ripple Rejection



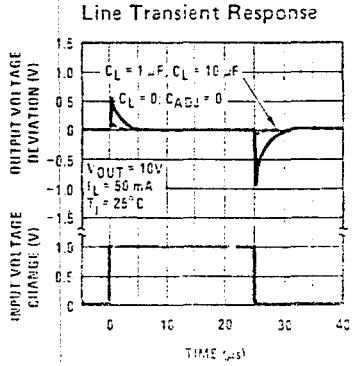
Ripple Rejection



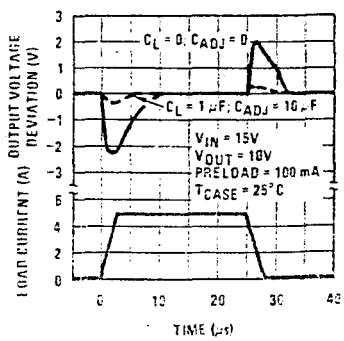
Ripple Rejection



Line Transient Response



Load Transient Response



Application Hints

In operation, the LM138 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$

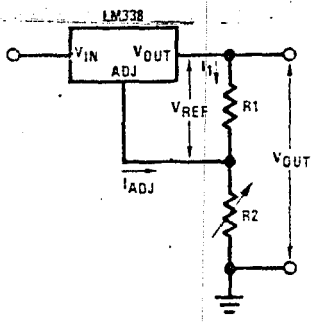


FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM138 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM138 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 75 dB ripple rejection is obtainable at any output level. Increases over 20 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may [illegible] than a 0.1 μF disc as a bypass.

Although the LM138 is stable with no outout capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM138 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

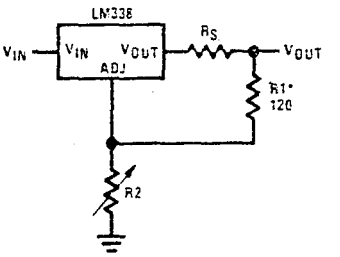


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

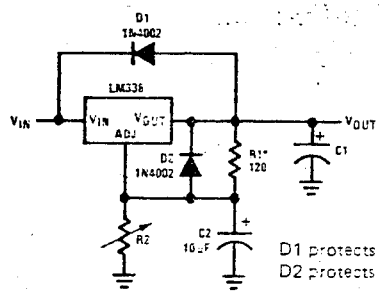
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM138 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive

Application Hints (Continued)

regulators. For output capacitors of 100 μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM138 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM138 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

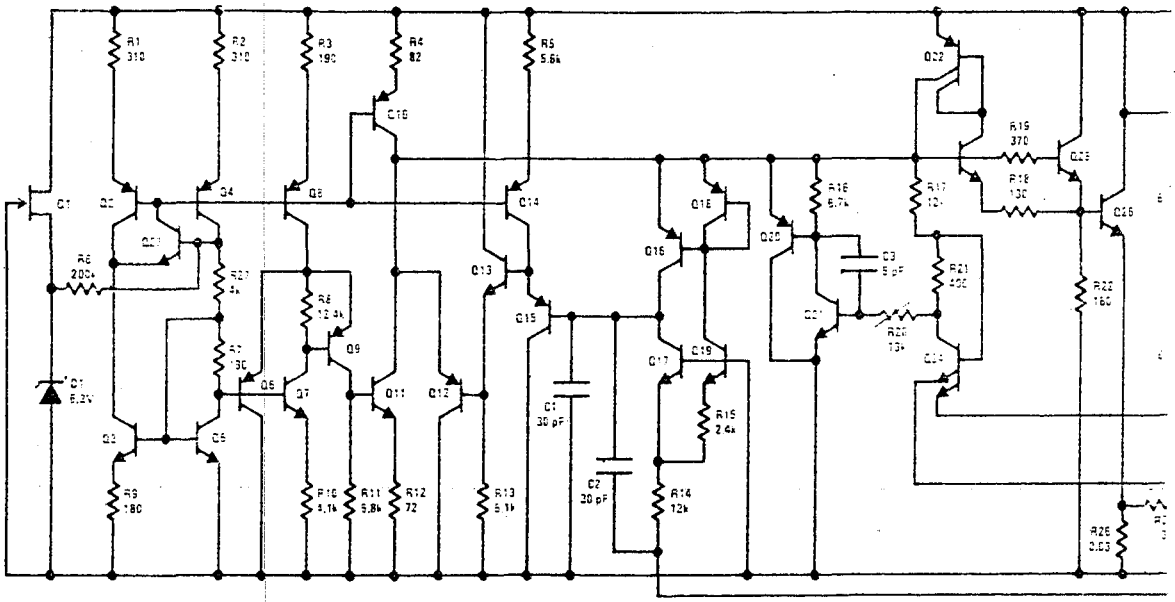


$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2I_A$$

*R1 = 240Ω for LM138 and LM238

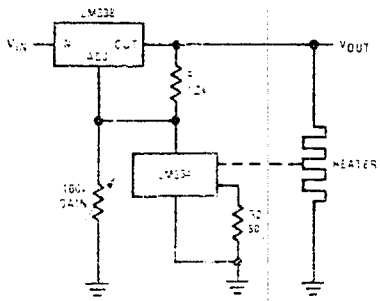
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

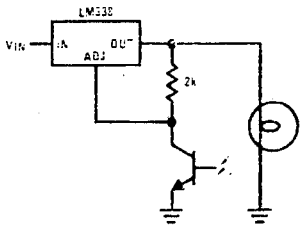


Typical Applications (Continued)

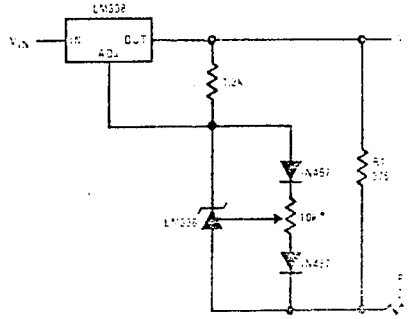
Temperature Controller



Light Controller



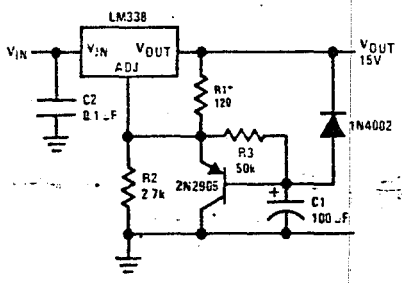
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

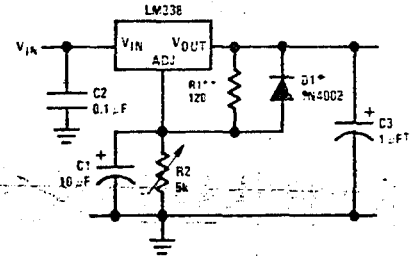
Typical Applications (Continued)

Slow Turn-ON 15V Regulator



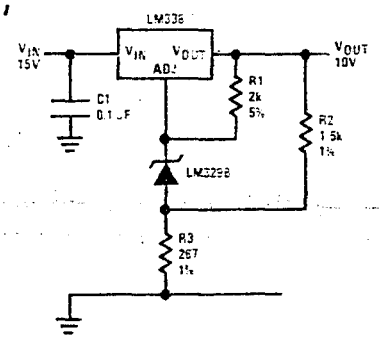
*R1 = 240Ω for LM138 and LM238

Adjustable Regulator with Improved Ripple Rejection

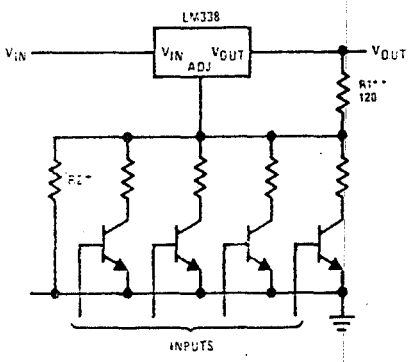


†Solid tantalum
*Discharges C1 if output is shorted to ground
**R1 = 240Ω for LM138 and LM238

High Stability 10V Regulator

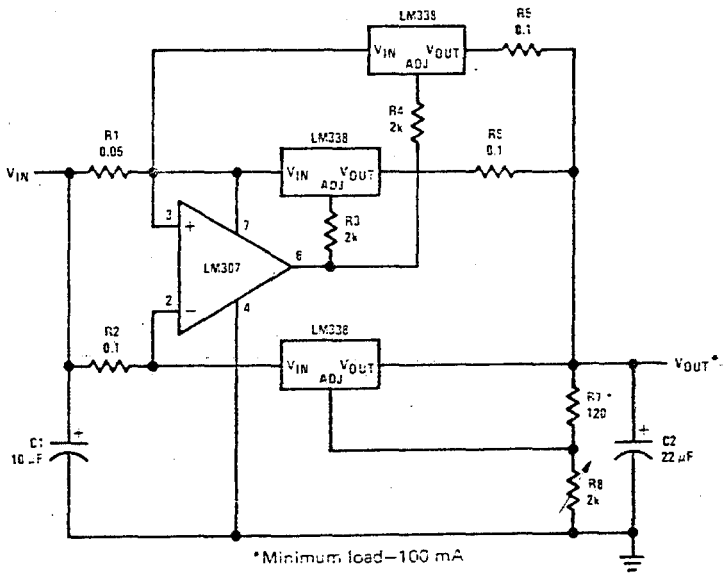


Digitally Selected Outputs



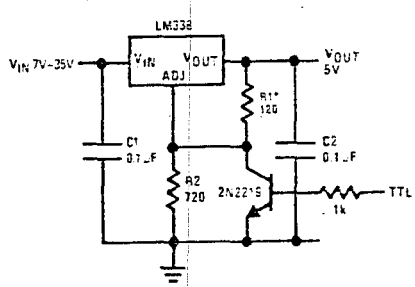
*Sets maximum VOUT
**R1 = 240Ω for LM138 and LM238

15A Regulator



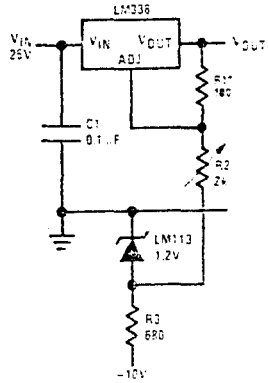
*Minimum load—100 mA

5V Logic Regulator with Electronic Shutdown**



*R1 = 240Ω for LM138 or LM238
†Minimum output ≈ 1.2V

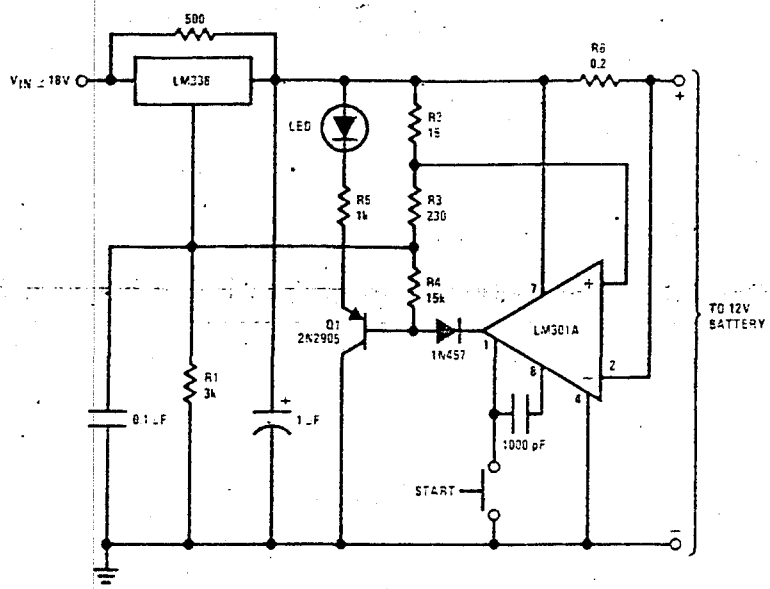
0 to 22V Regulator



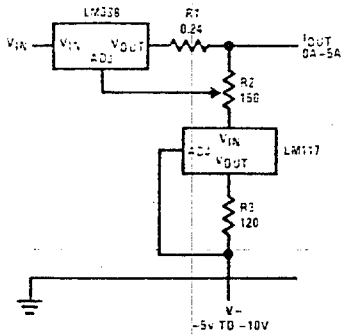
*R1=240Ω, R2 = 5k for LM138 and LM238

Typical Applications (Continued)

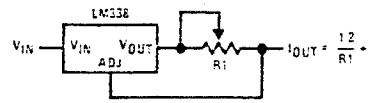
12V Battery Charger



Adjustable Current Regulator

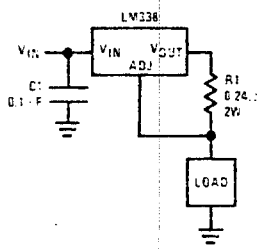


Precision Current Limiter

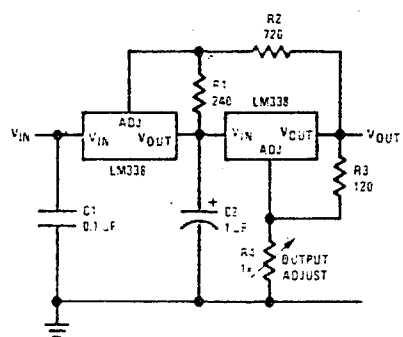


*$0.4 \leq R1 \leq 120\Omega$

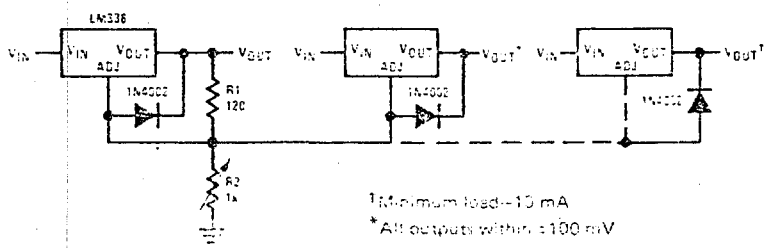
5A Current Regulator



Tracking Preregulator



Adjusting Multiple On-Card Regulators with Single Control*

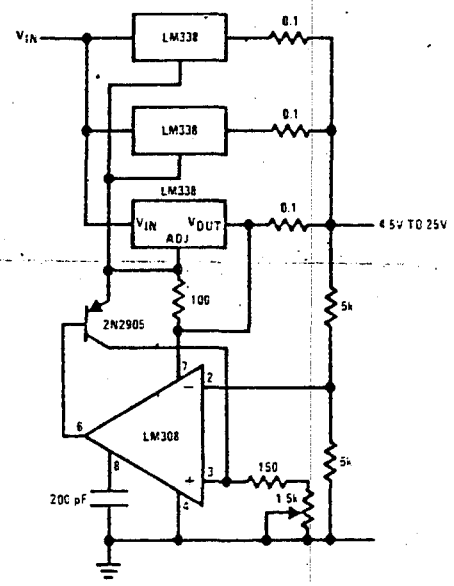


†Minimum load = 10 mA

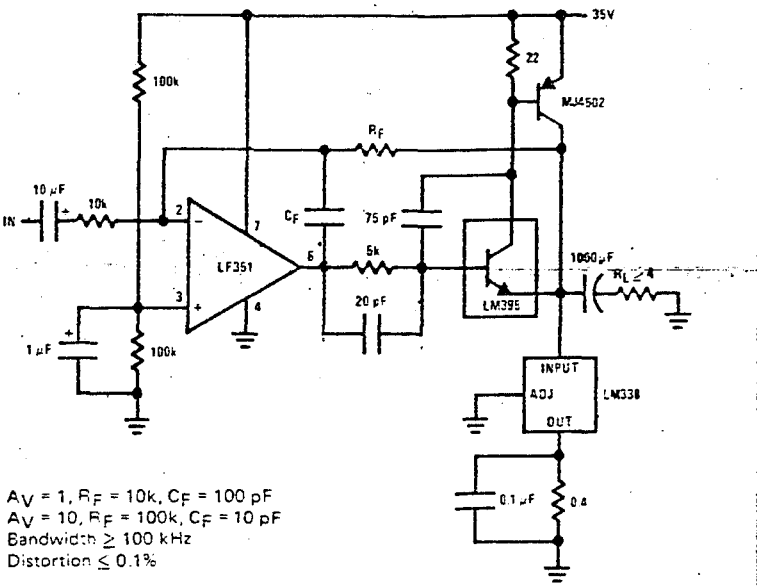
*All outputs within ±100 mV

Typical Applications (Continued)

Adjustable 15A Regulator

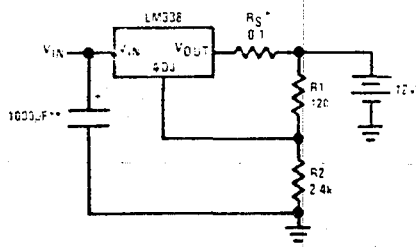


Power Amplifier



AV = 1, RF = 10k, CF = 100 pF
AV = 10, RF = 100k, CF = 10 pF
Bandwidth ≥ 100 kHz
Distortion ≤ 0.1%

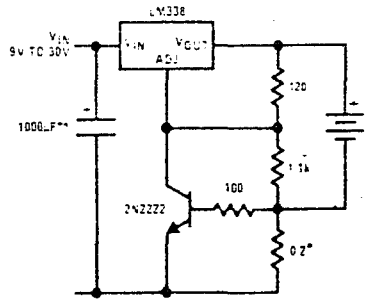
Simple 12V Battery Charger



*R_S—sets output impedance of charger $Z_{OUT} = R_S \left(1 + \frac{R2}{R1}\right)$
Use of R_S allows low charging rates with fully charged battery.

**The 1000 µF is recommended to filter out input transients

Current Limited 6V Charger

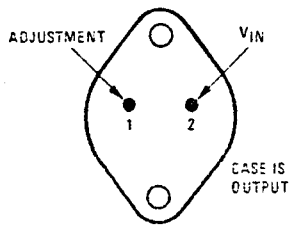


*Sets max charge current to 3A

**The 1000 µF is recommended to filter out input transients

Connection Diagram

Metal Can Package



BOTTOM VIEW

Order Number
LM138K STEEL
LM238K STEEL
LM338K STEEL
See NS Package K02A

National Semiconductor

A to D, D to A

MICRO-DAC™ DAC0830/0831/0832
8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DAC's (MICRO-DAC's™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

Micro-Dac is a trademark of National Semiconductor Corp.

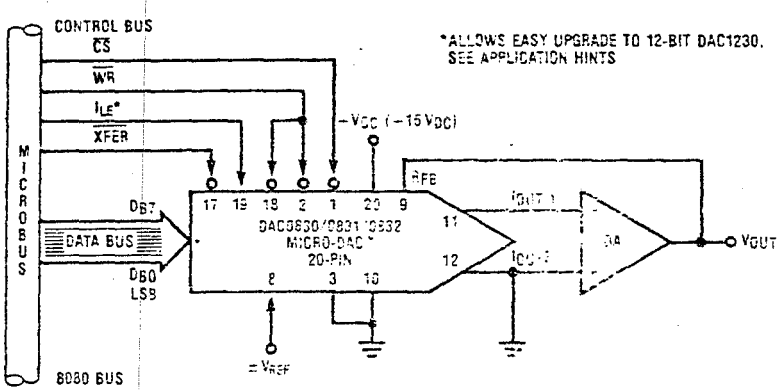
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full-scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired

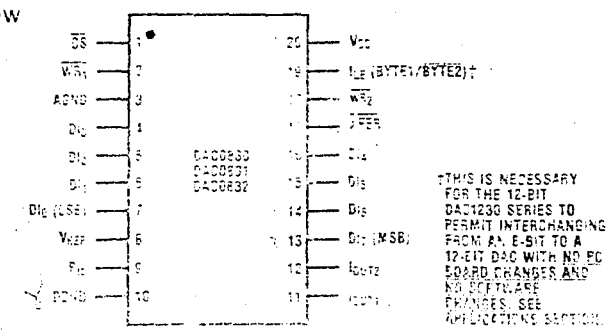
Key Specifications

■ Current settling time	1 μs
■ Resolution	8-bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application



Pin Configuration Top View



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at any digital input	V_{CC} to GND
Voltage at V_{REF} input	±25V
Storage temperature range	−65°C to +150°C
Package dissipation at T_A = 25°C (Note 3)	500 mW
DC voltage applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range	
Part numbers with 'LCN' suffix	
Part numbers with 'LCD' suffix	−40
Part numbers with 'LD' Suffix	−55
Voltage at any digital input	

General Electrical Characteristics T_A = 25°C, V_{REF} = 10.000 V_{DC} unless otherwise noted

Parameter	Conditions	See Note	V_{CC} = 12 V_{DC} ± 5% to 15 V_{DC} ± 5%			V_{CC} = 5 V_{DC} ± 5%		
			Min.	Typ.	Max.	Min.	Typ.	Max.
Resolution			8	8	8	8	8	8
Linearity Error	Zero and full scale adjusted	4,7						
	$T_{MIN} < T_A < T_{MAX}$	6						
	$-10V \leq V_{REF} \leq +10V$	5						
	DAC0830				0.05			0.05
	DAC0831				0.1			0.1
	DAC0832				0.2			0.2
Differential Nonlinearity	Zero and full scale adjusted	4,7						
	$T_{MIN} < T_A < T_{MAX}$	6						
	$-10V \leq V_{REF} \leq +10V$	5						
	DAC0830				0.1			0.1
	DAC0831				0.2			0.2
	DAC0832				0.4			0.4
Monotonicity	$T_{MIN} < T_A < T_{MAX}$	4,6						
	$-10V \leq V_{REF} \leq +10V$	5	8	8	8	8	8	8
Gain Error	Using internal R_{fb}							
	$-10V \leq V_{REF} \leq +10V$	5	−1.0	±0.2	1.0	−1.0	±0.2	1.0
Gain Error Tempco	$T_{MIN} < T_A < T_{MAX}$	6						
	Using internal R_{fb}	10		0.0002	0.0006		0.0002	0.0006
Power Supply Rejection	All digital inputs latched high							
	V_{CC} = 14.5V to 15.5V			0.0002				
	11.5V to 12.5V			0.0006				
	4.5V to 5.5V						0.0130	
Reference Input Resistance			10	15	20	10	15	20
Output Feedthrough Error	V_{REF} = 20 V_{P-P}, f = 100 kHz							
	All data inputs latched low							
	D Package	9		3			3	
	N Package			3			3	
Output Capacitance I_{OUT1}	All data inputs latched low			70			70	
I_{OUT2}				200			200	
I_{OUT1}	All data inputs latched high			200			200	
I_{OUT2}				70			70	
Supply Current Drain	$T_{MIN} \leq T_A \leq T_{MAX}$	6		1.2	2.0		1.2	2.0

General Electrical Characteristics $T_A = 25°C$, $V_{REF} = 10.000\,V_{DC}$ unless otherwise noted

Parameter		Conditions	See Note	$V_{CC} = 12V_{DC} \pm 5\%$ to $15V_{DC} \pm 5\%$			$V_{CC} = 5V_{DC} \pm 5\%$			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{OUT1}	$T_{MIN} \leq T_A \leq T_{MAX}$ All data inputs latched low	6 11			100			100	nA
	I_{OUT2}	All data inputs latched high				100			100	nA
Digital Input Voltages		$T_{MIN} \leq T_A \leq T_{MAX}$ Low Level	6							
		LD suffix				0.8			0.6	V_{DC}
		Parts with LCD or LCN suffix				0.8			0.8	V_{DC}
		High Level All Parts		2.0			2.0			V_{DC}
Digital Input Currents		$T_{MIN} \leq T_A \leq T_{MAX}$	6							
		Digital inputs < 0.8V			−50	−200		−50	−200	μA_{DC}
		Digital inputs > 2.0V			0.1	+10		0.1	+10	μA_{DC}
Current Settling Time	t_S	$V_{IL} = 0V$, $V_{IH} = 5V$			1.0			1.0		μs
Write and XFER Pulse Width	t_W	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	8	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	320	100		500	350		ns
Data Set Up Time	t_{DS}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Data Hold Time	t_{DH}	$V_{IL} = 0V$, $V_{IH} = 5V$ $T_A = 25°C$	10	90	50		300	200		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		90	60		350	260		ns
Control Set Up Time	t_{CS}	$V_{IL} = 0V$, $V_{IL} = 5V$, $T_A = 25°C$	10	320	60		320	250		ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		320	100		500	350		ns
Control Hold Time	t_{CH}	$V_{IL} = 0V$, $V_{IH} = 5V$, $T_A = 25°C$	10	10			10			ns
		$T_{MIN} \leq T_A \leq T_{MAX}$		10			10			ns

Note 1: *"Absolute Maximum Ratings"* are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these *"Absolute Maximum"* limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} - V_{REF}$. For example, if $V_{REF} = 10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed at $V_{REF} = \pm 10\,V_{DC}$ and $V_{REF} = \pm 1\,V_{DC}$.

Note 6: $T_{MIN} = 0°C$ and $T_{MAX} = 70°C$ for "LCN" suffix parts.
$T_{MIN} = -40°C$ and $T_{MAX} = 85°C$ for "LCD" suffix parts.
$T_{MIN} = -55°C$ and $T_{MAX} = 125°C$ for "LD" suffix parts.

Note 7: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)." This guarantees that after performing a zero and full scale adjustment (See Sections 2.5 and 2.6) the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

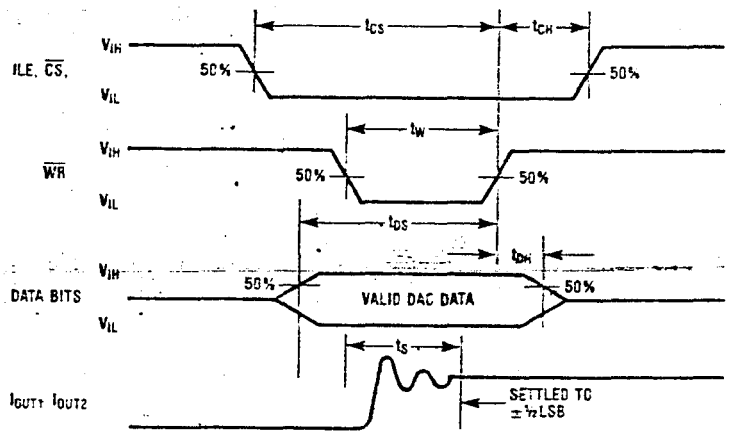
Note 8: This specification implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6 mV.

Note 10: Guaranteed by design but not tested.

Note 11: A 100 nA leakage current with $R_{fb} = 20k$ and $V_{REF} = 10V$ corresponds to a zero error of $(100 \times 10^{-9} \times 20 \times 10^3) \times 100/10$ which is 2% of FS.

Switching Waveforms:



Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: Input Latch Enable (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: Write 1. The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch — $\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: Write 2 (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: Transfer control signal (active low).The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: Digital Inputs. DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = cons$ scale for a fixed reference voltage).

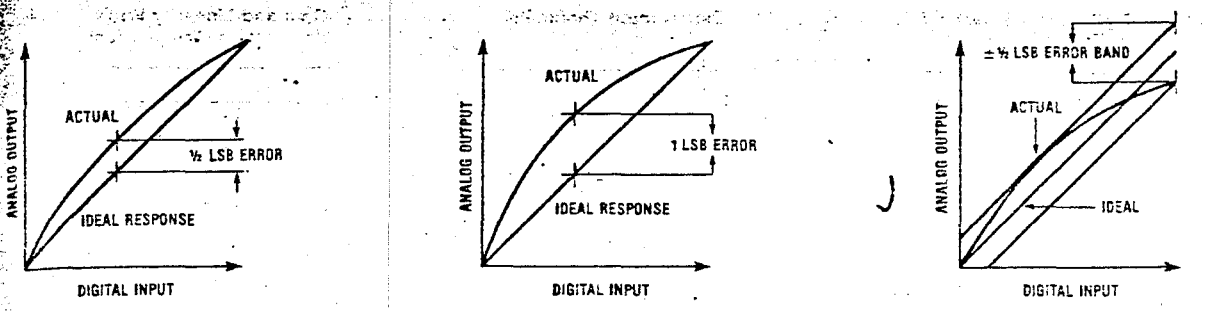
R_{fb}: Feedback Resistor. The feedback res vided on the IC chip for use as the s back resistor for the external op am used to provide an output voltage fc This on-chip resistor should always b an external resistor) since it matche tors which are used in the on-chip F and tracks these resistors over tem

V_{REF}: Reference Voltage Input. This input an external precision voltage source ternal R-2R ladder. V_{REF} can be sel the range of +10 to −10V. This is als log voltage input for a 4-quadrant r DAC application.

V_{CC}: Digital Supply Voltage. This is the po pin for the part. V_{CC} can be from +5 : Operation is optimum for $+15V_{DC}$.

AGND: Analog Ground. This is the grour analog circuitry. This pin must alwa nected to the digital ground potenti

DGND: Digital Ground. This is the ground fc tal logic.



a) End point test after zero and fs adj.

b) Best straight line

c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39\,mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

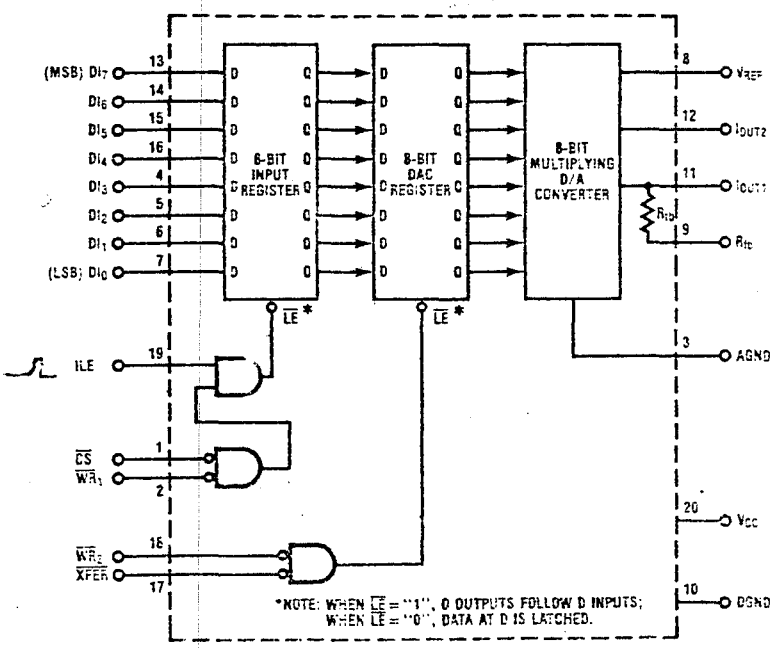
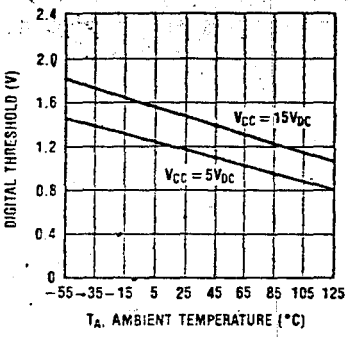
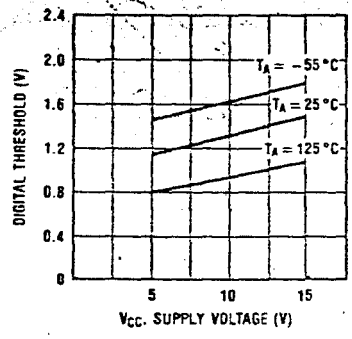


Figure 1. DAC0830 Functional Diagram

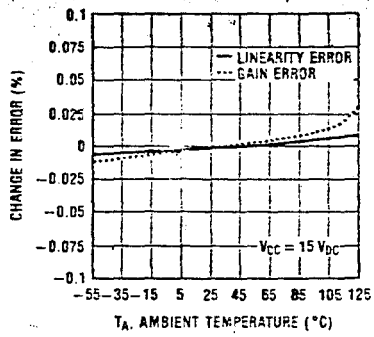
Digital Input Threshold vs. Temperature



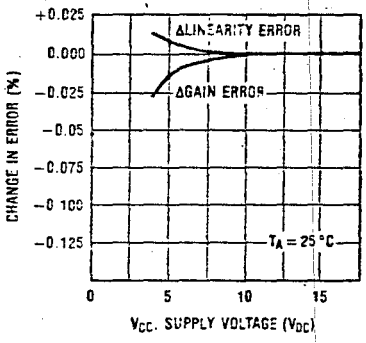
Digital Input Threshold vs. V_{CC}



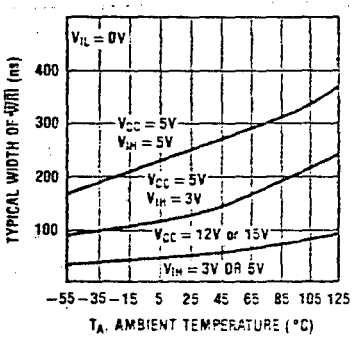
Gain and Linearity Error Variation vs. Temperature



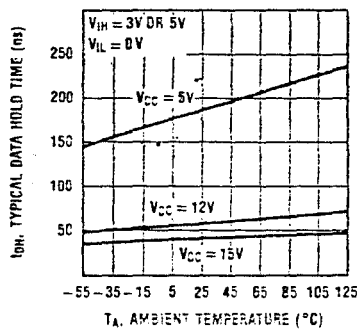
Gain and Linearity Error Variation vs. Supply Voltage



Typical Write Pulse Width



Typical Data Hold Time



DAC0830 Series Application Hints

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC™. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 Digital Considerations

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system updated to their new analog output levels simultane via a common strobe signal.

The timing requirements and logic level conventic the register control signals have been designed to mize or eliminate external interfacing logic when ap to most popular microprocessors and development tems. It is easy to think of these converters as "write only" memory locations that provide an ar output quantity. All inputs to these DAC's meet voltage level specs and can also be driven directly high voltage CMOS logic in non-microprocessor b systems. To prevent damage to the chip from static charge, all unused digital inputs should be tied to V ground. If any of the digital inputs are inadvertantl floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a do buffered manner is basically a two step or double operation. In a microprocessor system two unique tem addresses must be decoded, one for the input l controlled by the $\overline{CS}$ pin and a second for the DAC I which is controlled by the $\overline{XFER}$ line. If more than DAC is being driven, Figure 2, the $\overline{CS}$ line of each D would typically be decoded individually, but all of converters could share a common $\overline{XFER}$ address to a simultaneous updating of any number of DAC's. timing for this operation is shown, Figure 3.

It is important to note that the analog outputs that change after a simultaneous transfer are those from DAC's whose input register had been modified prio the $\overline{XFER}$ command.

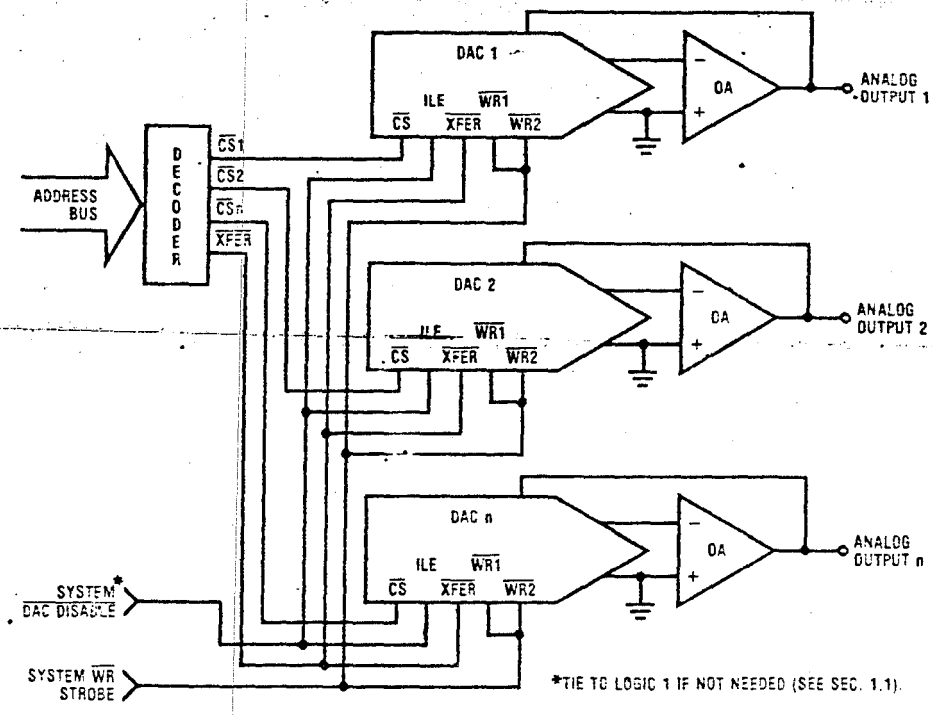


Figure 2. Controlling Multiple DAC's

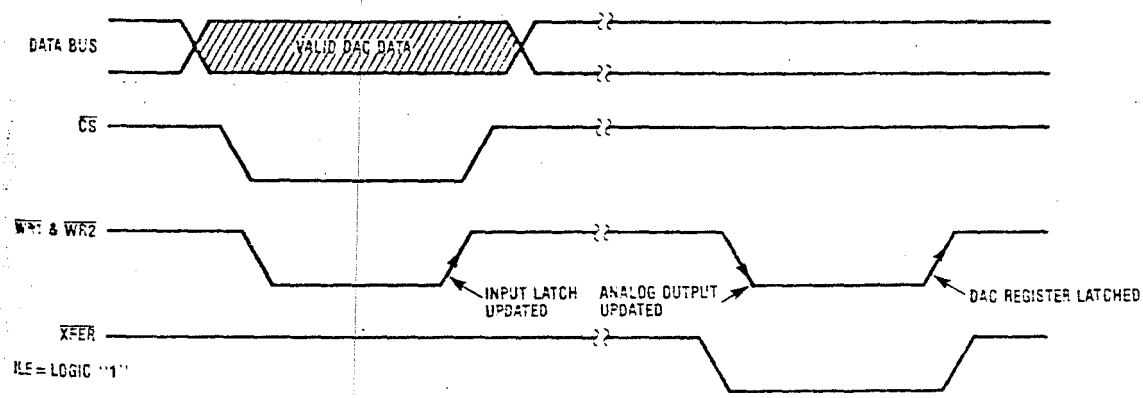


Figure 3.

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal CS signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling the line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in microprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

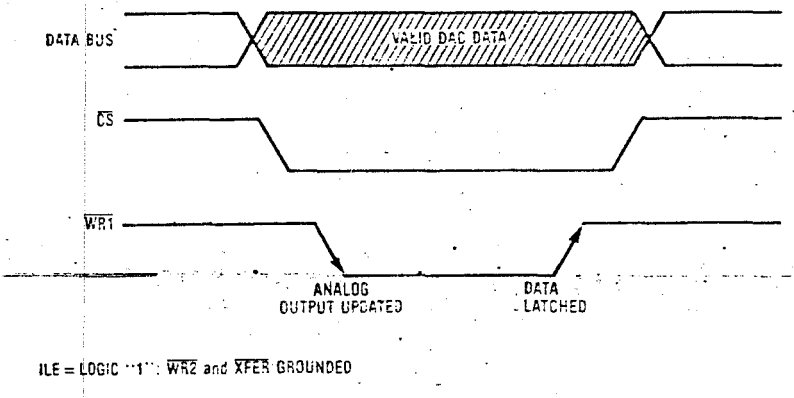


Figure 4.

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in figure 4.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC's to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 500 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 100 ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data is latched. This hold time is defined as the length of data must be held valid on the digital inputs *after* a fied (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high trans latch the applied data.

If the controlling device or system does not inh meet these timing specs the DAC can be treate slow memory or peripheral and utilize a techni extend the write strobe. A simple extension of th time, by adding a wait state, can simultaneously h write strobe active and data valid on the bus to the minimum $\overline{WR}$ pulsewidth. If this does not pro sufficient data hold time at the end of the write c negative edge triggered one-shot can be includ tween the system write strobe and the $\overline{WR}$ pin DAC. This is illustrated in Figure 5 for an exampla tem which provides a 250 ns $\overline{WR}$ strobe time with hold time of only 10 ns.

The proper data set-up time prior to the latching ec to HI transition) of the $\overline{WR}$ strobe, is insured if t pulsewidth is within spec and the data is valid bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, t digital inputs are changing state, a narrow spike rent may flow out of the current output terminal spike is caused by the rapid switching of interna gates that are responding to the input changes.

There are several recommendations to minimize t fect. When latching data in the DAC, always use th register as the latch. Second, reducing the V_{CC} for the DAC from +15 volts to the +5V offers a fa 5 improvement in the magnitude of the feedthrou at the expense of internal logic switching speed. F increasing C_C (Figure 8) to a value consistent w actual circuit bandwidth requirements can pro substantial damping effect on any output spik-s

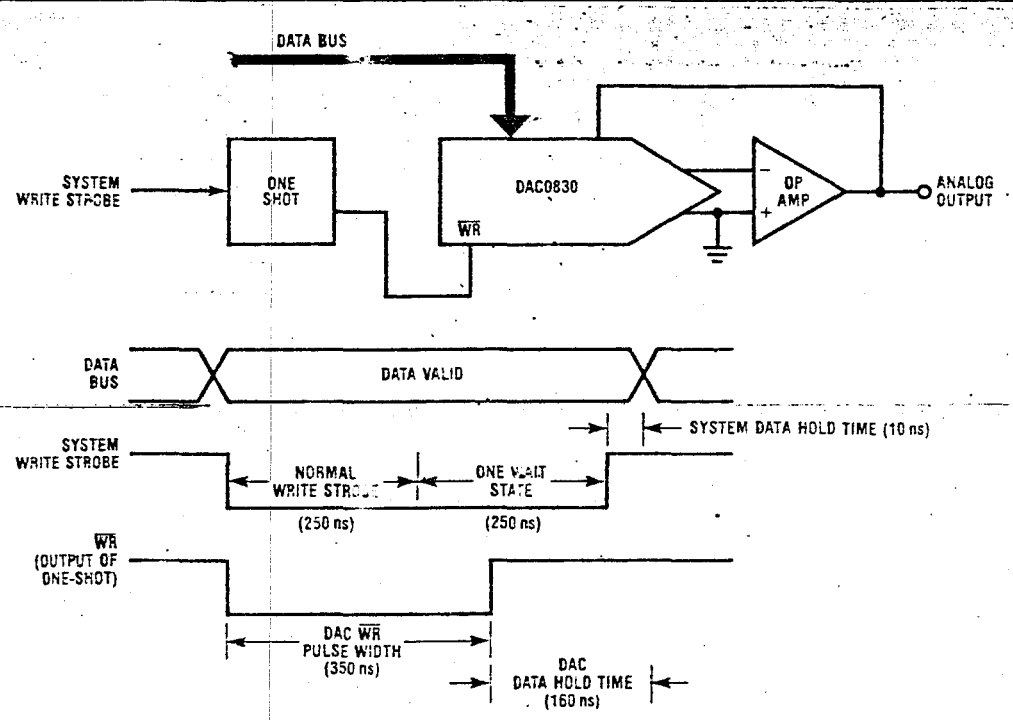


Figure 5. Accommodating a High Speed System

2.0 Analog Considerations

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, Figure 6, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in Figure 6. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in Figure 7.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage souce or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

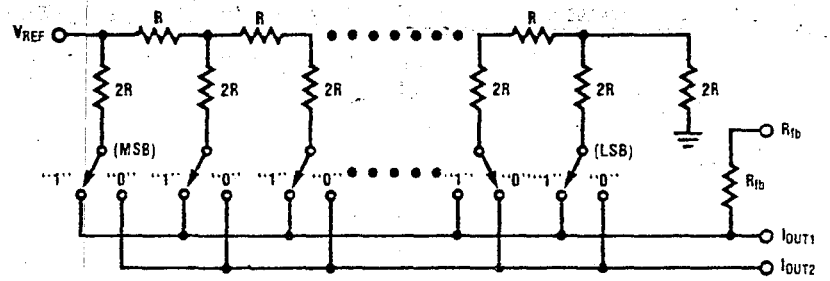


Figure 6.

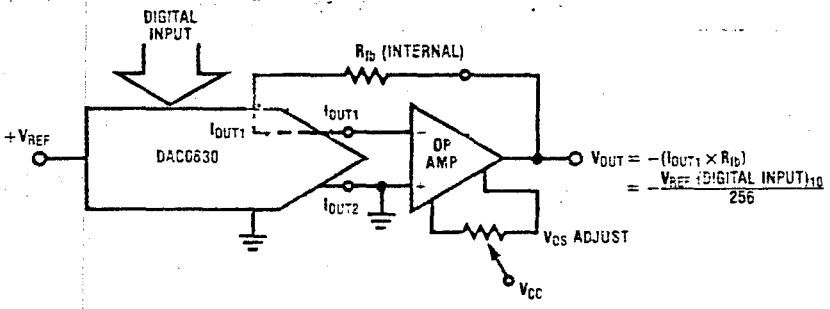


Figure 7.

2.3 Op Amp Considerations

The op amp used in Figure 7 should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™* op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in Figure 8, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

*BI-FET is a trademark of National Semiconductor Corporation.

2.4 Bipolar Output Voltage with a Fixed Reference

The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows four-quadrant multiplication of the reference voltage.

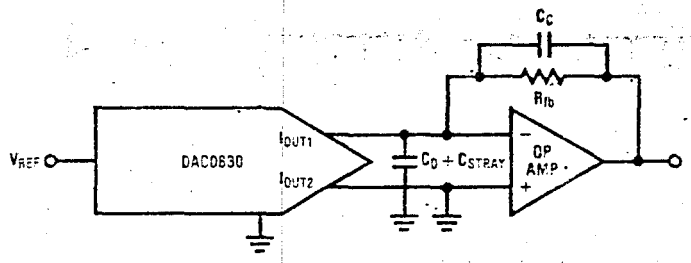
The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm D$ Code $= \mp V_{OUT}$. This circuit is shown in Figure 9.

This configuration features several improvements existing circuits for bipolar outputs with other mul ing DAC's. Only the offset voltage of amplifier 1 h be nulled to preserve linearity of the DAC. The c voltage error of the second op amp (although a cons output voltage error) has no effect on linearity. It sh be nulled only if absolute output accuracy is requ Finally, the values of the resistors around the se amplifier do not have to match the internal DAC resis they need only to match and temperature track other. A thin film 4-resistor network available from man Instruments, Inc. (part no. 694-3-R10K-D) is ic suited for this application. These resistors are ma to 0.1% and exhibit only 5 ppm/°C resistance tra tempco. Two of the four available 10 kΩ resistors c paralleled to form R in Figure 9 and the other two c used independently as the resistances labeled 2F

2.5 Zero Adjustment

For accurate conversions, the input offset voltage output amplifier must always be nulled. Amplifier c errors create an overall degradation of DAC linea

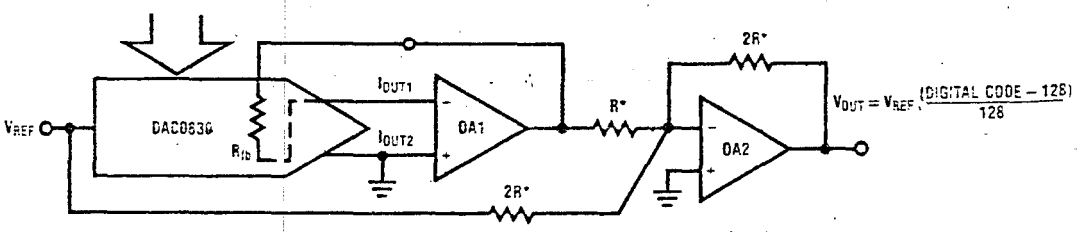
The fundamental purpose of zeroing is to make the age appearing at the DAC outputs as near $0V_{DC}$ as sible. This is accomplished for the typical DAC amp connection (Figure 7) by shorting out R_{fb}, the lifier feedback resistor, and adjusting the V_{OS} n potentiometer of the op amp until the output reads volts. This is done, of course, with an applied c code of all zeros if I_{OUT1} is driving the op amp (all for I_{OUT2}). The short around R_{fb} is then removed ar converter is zero adjusted.



OP AMP	C_C	t_s (0 TO FULL SCALE)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*2.4kΩ RESISTOR ADDED FROM (−) INPUT TO GROUND TO INSURE STABILITY

Figure 8.



*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

INPUT CODE	IDEAL V_{OUT}	
MSB . . . LSB	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1\,LSB$	$-\|V_{REF}\| + 1\,LSB$
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\|V_{REF}\|/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	$-1\,LSB$	$+1\,LSB$
0 0 1 1 1 1 1 1	$-\frac{\|V_{REF}\|}{2} - 1\,LSB$	$\frac{\|V_{REF}\|}{2} + 1\,LSB$
0 0 0 0 0 0 0 0	$-\|V_{REF}\|$	$+\|V_{REF}\|$

Figure 9.

2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in Figure 10 to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error tempco by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in Figure 10, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error tempco would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in Figure 11.

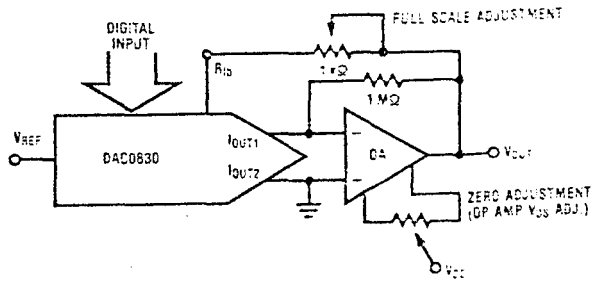


Figure 10. Adding Full-Scale Adjustment

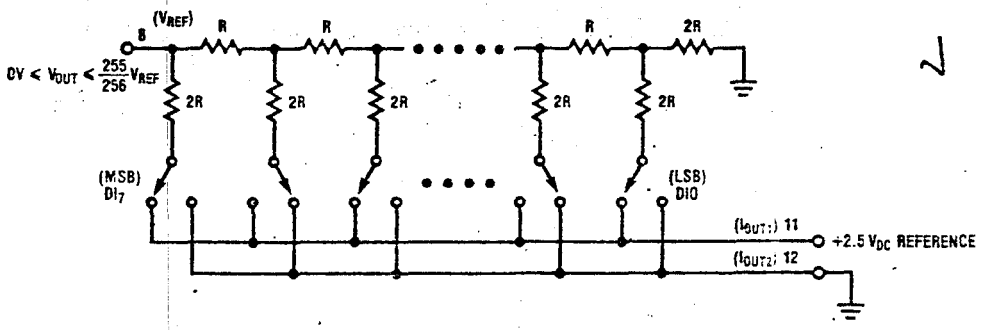
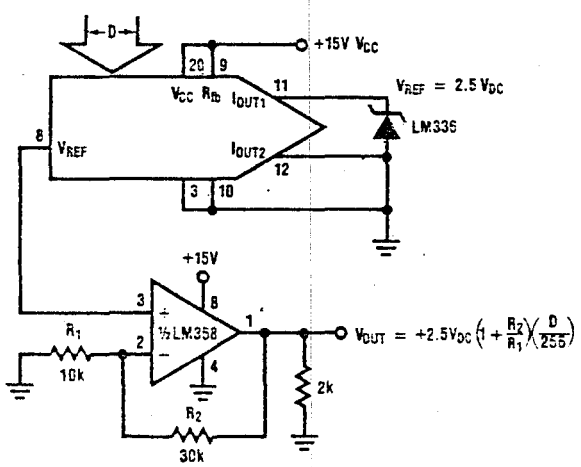


Figure 11. Voltage Mode Switching

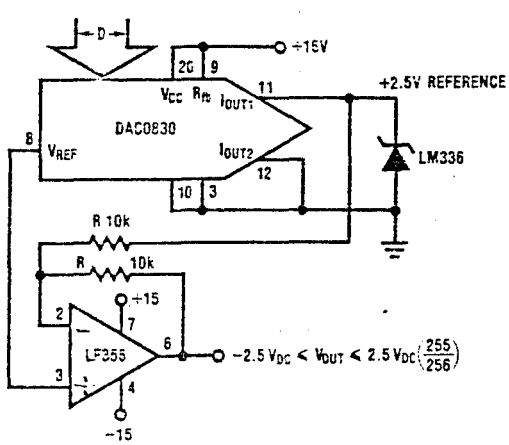
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in Figures 12, 13, 14 and 15.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drop requirements of the ladder switches. To insure that the switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5\,V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions insure less than 0.1% linearity and gain error change. Figures 16, 17 and 18 characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

Figure 12. Single Supply DAC



- $V_{OUT} = 2.5\,V\left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

Figure 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

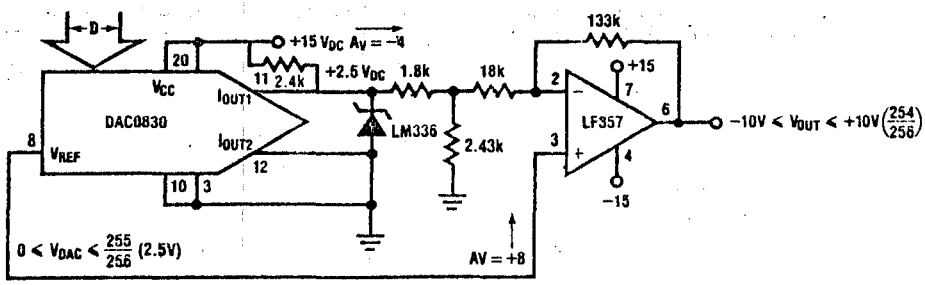
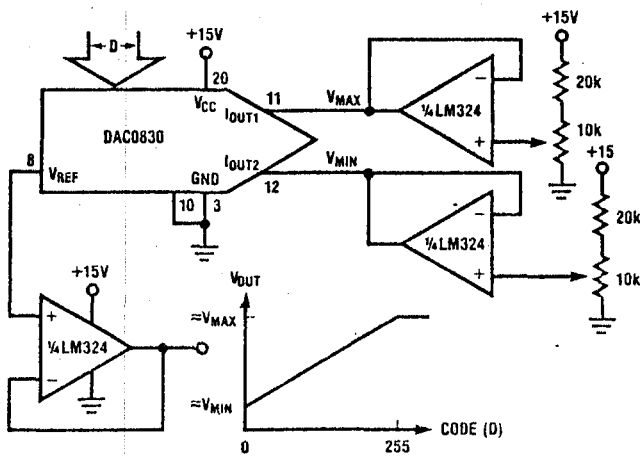


Figure 14. Bipolar Output with Increased Output Voltage Swing



- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be ≤ +5VDC and ≥ 0V.
- Incremental Output Step = $\frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

Figure 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

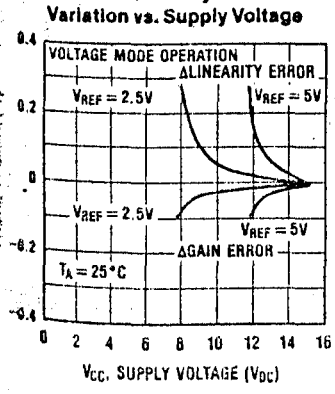


Figure 16.

Gain and Linearity Error Variation vs. Reference Voltage

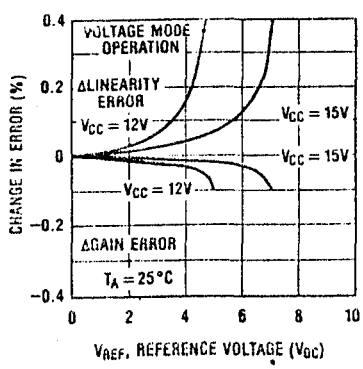


Figure 17.

Gain and Linearity Error Variation vs. Temperature

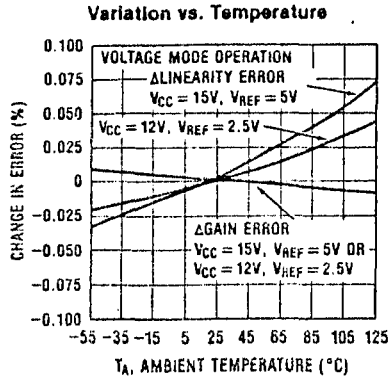


Figure 18.

NOTE: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

2.8 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DAC's.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will typically cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertent noise from appearing on the analog output.

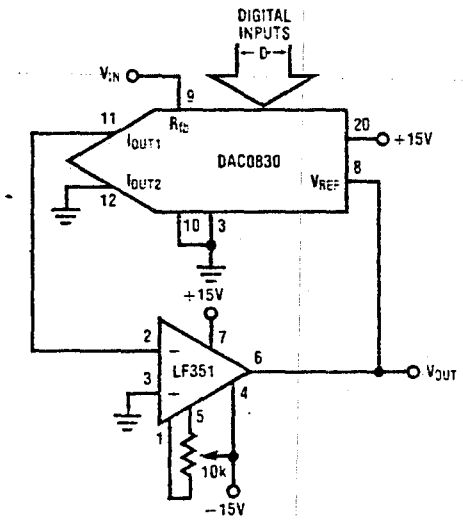
Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

3.0 General Application Ideas

The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

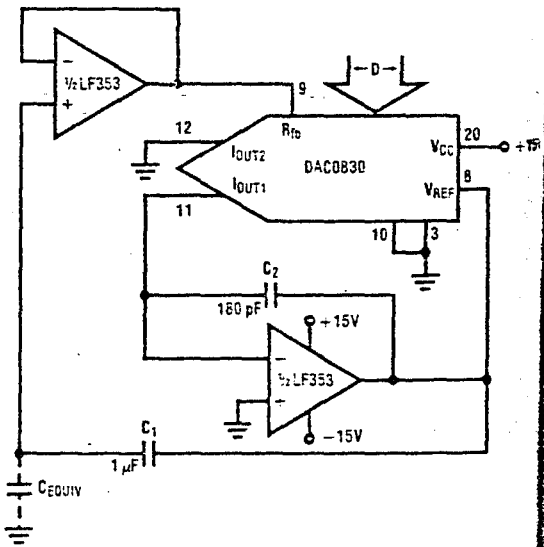
The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input Pin 13 MSB	Pin 7 LSB	D Decimal Equivalent
1 1 1 1 1 1 1 1		255
1 0 0 0 0 0 0 0		128
0 0 0 1 0 0 0 0		16
0 0 0 0 0 0 1 0		2
0 0 0 0 0 0 0 0		0



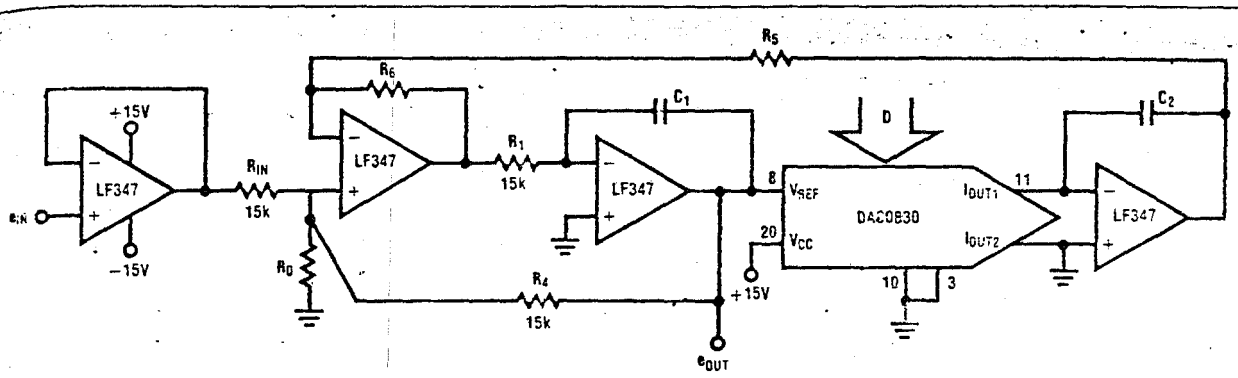
DAC Controlled Amplifier (Volume Control)

- $V_{OUT} = \frac{-V_{IN}\,(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.



Capacitance Multiplier

- $C_{EQUIV} = C_1\left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\ (\text{op amp})}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.

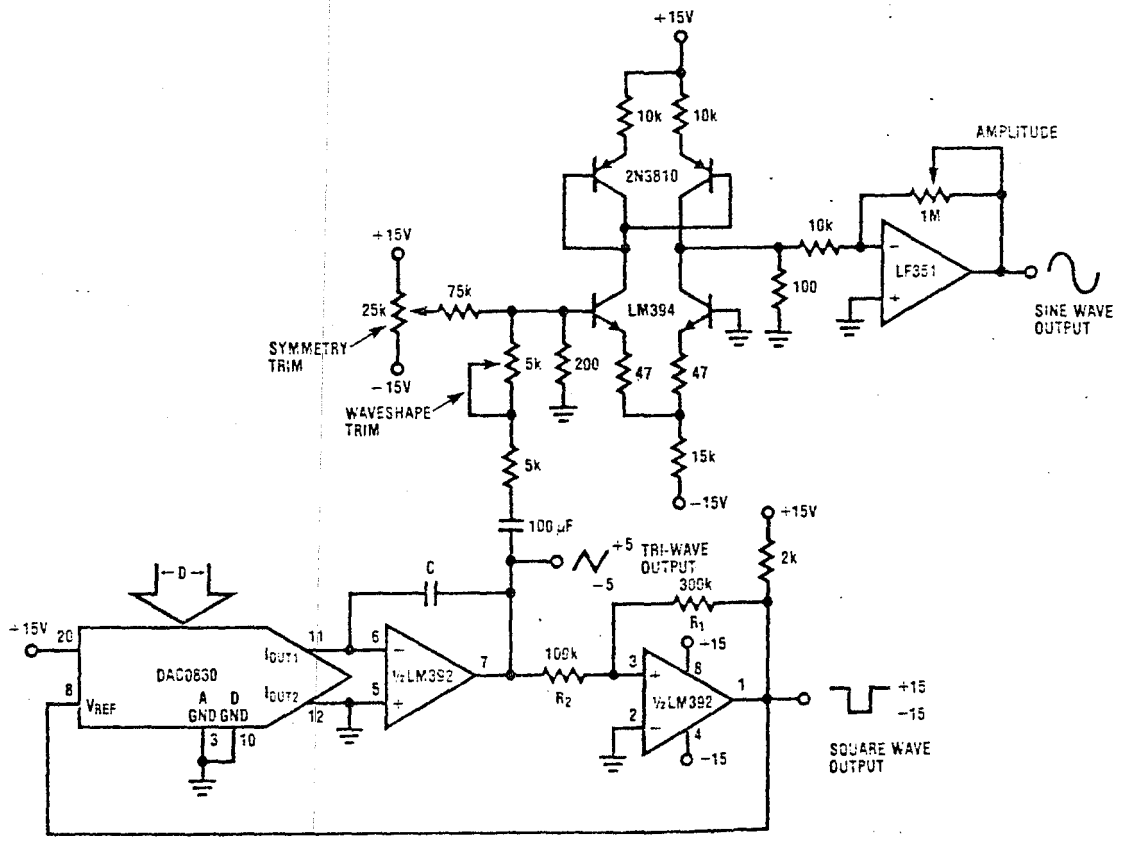


Variable f_O, Variable Q_O, Constant BW Bandpass Filter

- $f_O = \frac{\sqrt{\frac{K\,D}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\frac{K\,D}{256}} \frac{(2R_O + R_1)}{R_O(K+1)}$; $3\,\text{db BW} = \frac{R_O(K+1)}{2\pi R_1 C(2R_O + R_1)}$

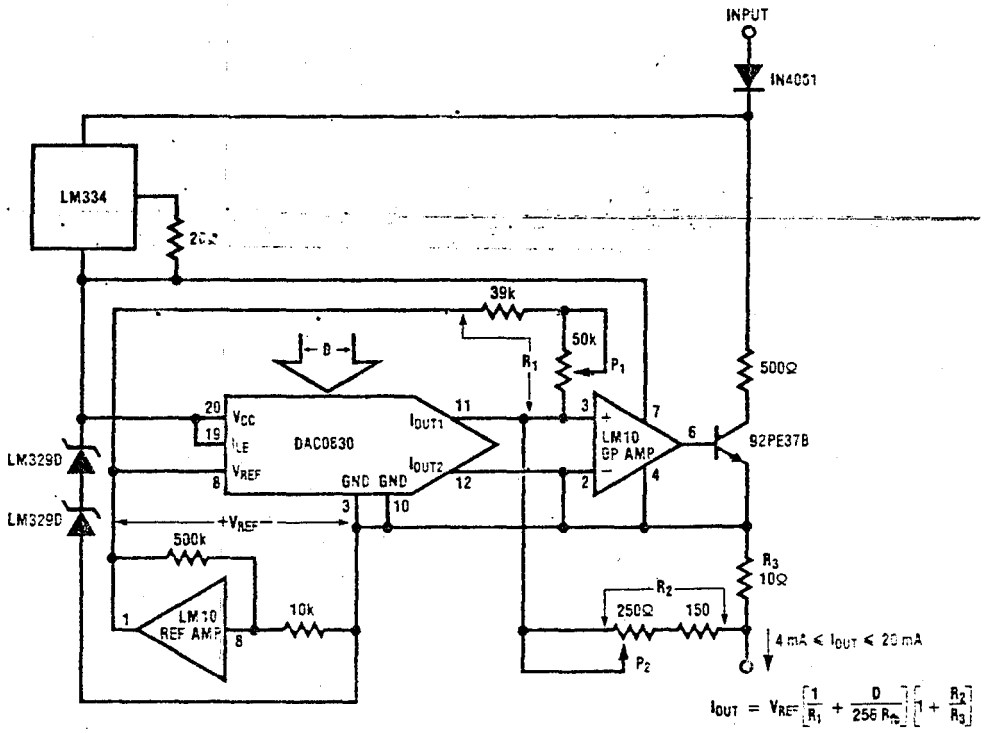
  where $C_1 = C_2 = C$; $K = \frac{R_6}{R_5}$ and $R_1 = R$ of DAC = 15k

- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ≤ 200 kHz.



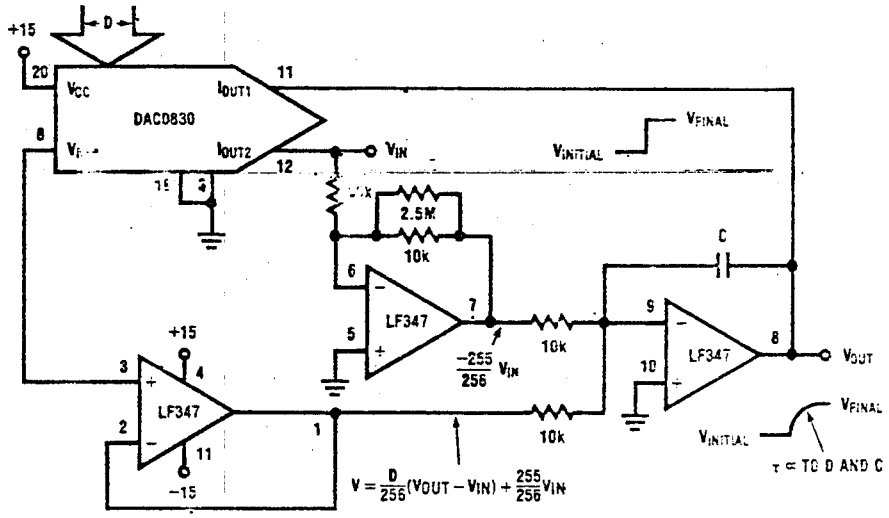
DAC Controlled Function Generator

- DAC controls the frequency of sine, square, and triangle outputs
- $f = \frac{D}{256(120k)C}$ for $V_{OMAX} = V_{OMIN}$ of square wave output and $R_1 = 3R_2$
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and waveshape for minimum sine wave distortion.



Two Terminal Floating 4 to 20 mA Current Loop Controller

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D = 0) to 19.94 mA (for D = 255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).



DAC Controlled Exponential Time Response

- Output responds exponentially to input changes and automatically stops when $V_{OUT} = V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

National Semiconductor

A to D, D to A

ADC0800 8-Bit A/D Converter

General Description

The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

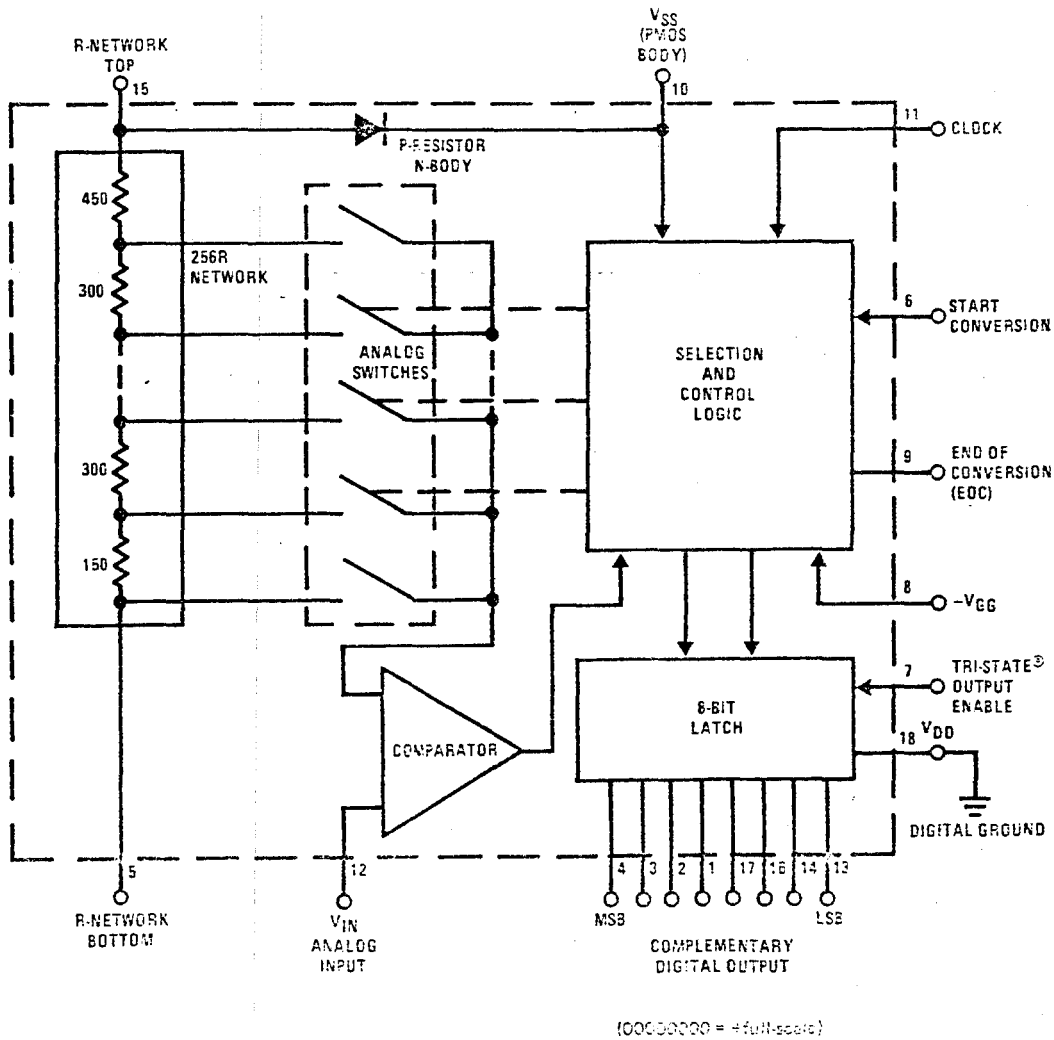
The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast — T_C = 50 μs
- Contains output latches
- TTL compatible

Supply voltages	5 V_{DC} and −12 V_{DC}
Resolution	8 bits
Linearity	±1 LSB
Conversion speed	40 clock periods
Clock range	50 to 800 kHz

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD})	V_{SS}–22V
Supply Voltage (V_{GG})	V_{SS}–22V
Voltage at Any Input	V_{SS} + 0.3V to V_{SS}–22V
Storage Temperature	150°C
Operating Temperature	
ADC0800PD	–55°C to +125°C
ADC0800PCD	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

These specifications apply for V_{SS} = 5.0 V_{DC}, V_{GG} = –12.0 V_{DC}, V_{DD} = 0 V_{DC}, a reference voltage of 10.000 V_{DC} acr the on-chip R-network ($V_{R\text{-}NETWORK\ TOP}$ = 5.000 V_{DC} and $V_{R\text{-}NETWORK\ BOTTOM}$ = –5.000 V_{DC}) and a clock f quency of 800 kHz. For all tests, a 475Ω resistor is used from pin 5 to ground. Unless otherwise noted, these specifications ap over an ambient temperature range of –55°C to +125°C for the ADC0800PD and 0°C to +70°C for the ADC0800PCD.

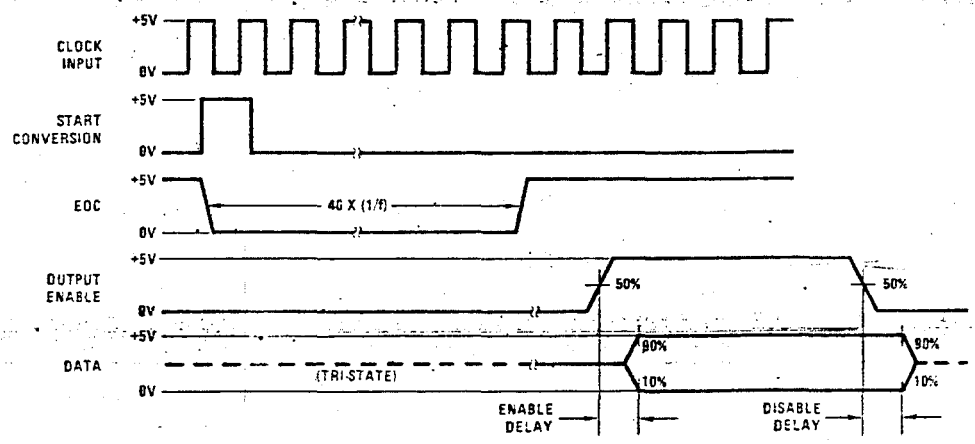
PARAMETER	CONDITIONS	MIN	TYP	MAX	UI
Non-Linearity	T_A = 25°C, (Note 1)			±1	
	Over Temperature, (Note 1)			±2	
Differential Non-Linearity				±1/2	
Zero Error				±2	
Zero Error Temperature Coefficient	(Note 2)			0.01	
Full-Scale Error				±2	
Full-Scale Error Temperature Coefficient	(Note 2)			0.01	
Input Leakage				1	
Logical "1" Input Voltage	All Inputs	V_{SS}–1.0		V_{SS}	
Logical "0" Input Voltage	All Inputs	V_{GG}		V_{SS}–4.2	
Logical Input Leakage	T_A = 25°C, All Inputs, V_{IL} = V_{SS} – 10V			1	
Logical "1" Output Voltage	All Outputs, I_{OH} = 100 μA	2.4			
Logical "0" Output Voltage	All Outputs, I_{OL} = 1.6 mA			0.4	
Disabled Output Leakage	T_A = 25°C, All Outputs, V_{OL} = V_{SS} @ 10V			2	
Clock Frequency	0°C ≤ T_A ≤ +70°C	50		800	
	–55°C ≤ T_A ≤ +125°C	100		500	
Clock Pulse Duty Cycle		40		60	
TRI-STATE Enable/Disable Time				1	
Start Conversion Pulse	(Note 3)	1		3 1/2	
					F
Power Supply Current	T_A = 25°C			20	

Note 1: Non-linearity specifications are based on best straight line.

Note 2: Guaranteed by design only.

Note 3: Start conversion pulse duration greater than 3 1/2 clock periods will cause conversion errors.

Timing Diagram



Data is complementary binary (full scale is all "0's" output).

Application Hints

OPERATION

The ADC0800 contains a network with 256-300Ω resistors in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference (10.00V) is applied across this network of 256 resistors. An analog input (V_{IN}) is first compared to the center point of the ladder via the appropriate switch. If V_{IN} is larger than $V_{REF}/2$, the internal logic changes the switch points and now compares V_{IN} and 3/4 V_{REF}. This process, known as successive approximation, continues until the best match of V_{IN} and V_{REF}/N is made. N now defines a specific tap on the resistor network. When the conversion is complete, the logic loads a binary word corresponding to this tap into the output latch and an end of conversion (EOC) logic level appears. The output latches hold this data valid until a new conversion is completed and new data is loaded into the latches. The data transfer occurs in about 200 ns so that valid data is present virtually all the time. Conversion requires 40 clock periods. The device may be operated in the free running mode by connecting the Start Conversion line to the End of Conversion line. However, to ensure start-up under all possible conditions, an external Start Conversion pulse is required during power up conditions.

REFERENCE

The reference applied across the 256 resistor network determines the analog input range. V_{REF} = 10.00V with the top of the R-network connected to 5V and the bottom connected to −5V gives a ±5V range. The reference can be level shifted between V_{SS} and V_{GG}. However, the voltage, which is applied to the top of the R-network (pin 15), must not exceed V_{SS} to prevent forward biasing the on-chip parasitic silicon diode which exists between the P-diffused resistors (pin 15) and the N-type body (pin 10, V_{SS}). Use of a standard logic power supply for V_{SS} can cause problems, both due to initial voltage tolerance and changes over temperature. A solution is to power the V_{SS} line (15 mA max drain) from the output of the op amp which is used to bias the top of the R-network (pin 15). The analog input voltage and the voltage which is applied to the bottom of the R-network (pin 5) must be at least 7V above the $-V_{DD}$ supply voltage to insure adequate voltage drive to the analog switches.

Other reference voltages may be used (such as 10.24V). If a 5V reference is used, the analog range will be 5V and accuracy will be reduced by a factor of 2. Thus, for maximum accuracy, it is desirable to operate with at least a 10V reference. For TTL logic levels, this requires 5V and −5V for the R-network. CMOS can operate at the 10 V_{DC} V_{SS} level and a single 10 V_{DC} reference can be used. All digital voltage levels for both inputs and outputs will be from ground to V_{SS}.

ANALOG INPUT AND SOURCE RESISTANCE CONSIDERATIONS

The lead to the analog input (pin 12) should be kept as short as possible. Both noise and digital clock coupling to this input can cause conversion errors. To minimize any input errors, the following source resistance considerations should be noted:

For $R_S \leq 5k$	No analog input bypass capacitor required, although a 0.1 μF input bypass capacitor will prevent pick-up due to unavoidable series lead inductance.
For $5k < R_S \leq 20k$	A 0.1 μF capacitor from the input (pin 12) to ground should be used.
For $R_S > 20k$	Input buffering is necessary.

If the overall converter system requires lowpass filtering of the analog input signal, use a 20 kΩ or less series resistor for a passive RC section or add an op amp RC active lowpass filter (with its inherent low output resistance) to insure accurate conversions.

CLOCK COUPLING

The clock lead should be kept away from the analog input line to reduce coupling.

LOGIC INPUTS

The logical "1" input voltage sv[illegible] for the Clock, Start Conversion and Output Enable[illegible] ld be (V_{SS} − 1.0V).

Application Hints (Continued)

CMOS will satisfy this requirement but a pull-up resistor should be used for TTL logic inputs.

RE-START AND DATA VALID AFTER EOC

The EOC line (pin 9) will be in the low state for a maximum of 40 clock periods to indicate "busy". A START pulse which occurs while the A/D is BUSY will reset the SAR and start a new conversion with the EOC signal remaining in the low state until the end of this new conversion. When the conversion is complete, the EOC line will go to the high voltage state. An additional 4 clock periods must be allowed to elapse after EOC goes high, before a new conversion cycle is requested. Start Conversion pulses which occur during this last 4 clock period interval may be ignored (see *Figures 1 and 2* for high speed operation). This is only a problem for high conversion rates and keeping the number of conversions per second less than (1/44) x f_{CLOCK} automatically guarantees proper operation. For example, for an 800 kHz clock, 18,000 conversions per second are allowed. The transfer of the new digital data to the output is initiated when EOC goes to the high voltage state.

POWER SUPPLIES

Standard supplies are V_{SS} = 5V, V_{GG} = −12V and V_{DD} = 0V. Device accuracy is dependent on stability of the reference voltage and has slight sensitivity to $V_{SS} - V_{GG}$. V_{DD} has no effect on accuracy. Noise spikes on the V_{SS} and V_{GG} supplies can cause improper conversion; therefore, filtering each supply with a 4.7 μF tantalum capacitor is recommended.

CONTINUOUS CONVERSIONS AND LOGIC CONTROL

Simply tying the EOC output to the Start Conversion input will allow continuous conversions, but an oscillation on this line will exist during the first 4 clock periods after EOC goes high. Adding a D flip-flop between EOC (D input) to Start Conversion (Q output) will prevent the oscillation and will allow a stop/continuous control via the "clear" input.

To prevent missing a start pulse which may occur after EOC goes high and prior to the required 4 clock period time interval, the circuit of *Figure 1* can be used. The RS latch can be set at any time and the 4-stage shift register delays the application of the start pulse to the A/D by 4 clock periods. The RS latch is reset 1 clock period after the A/D EOC signal goes to the low voltage state. This circuit also provides a Start Conversion pulse to the A/D which is 1 clock period wide.

A second control logic application circuit is shown in *Figure 2*. This allows an asynchronous start pulse of arbitrary length less than T_C, continuously converts for a fixed high level and provides a single clock period start pulse to the A/D. The binary counter is loaded with a count of 11 when the start pulse to the A/D appears. Counting is inhibited until the EOC signal from the A/D goes high. A carry pulse is then generated 4 clock periods after EOC goes high and is used to reset the input RS latch. This carry pulse can be used to indicate that the conversion is complete, the data has transferred to the output buffers and the system is ready for a new conversion cycle.

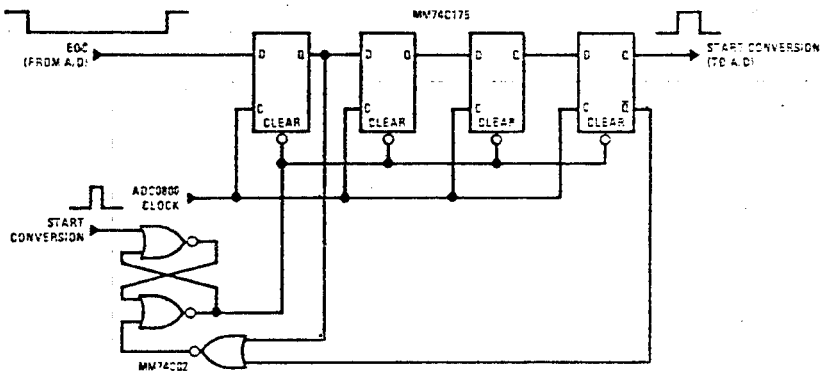


FIGURE 1. Delaying an Asynchronous Start Pulse

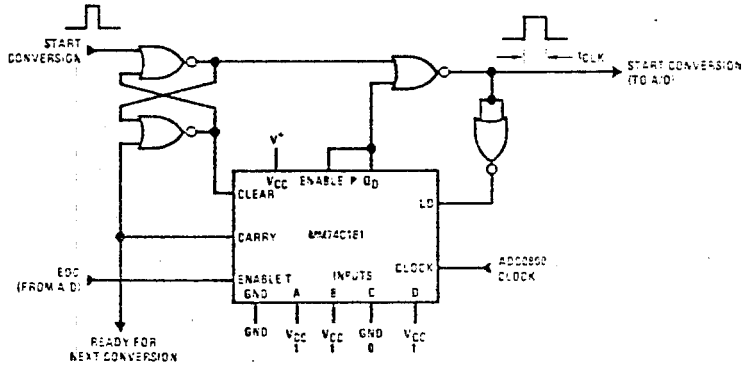


FIGURE 2. A/D Control Logic

Application Hints (Continued)

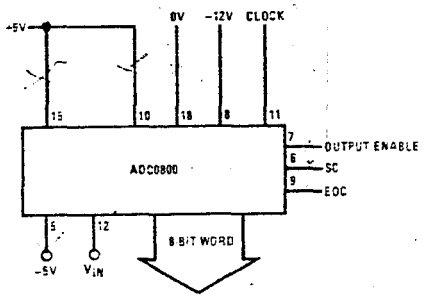
ZERO AND FULL-SCALE ADJUSTMENT

Zero Adjustment: This is the offset voltage required at the bottom of the R-network (pin 5) to make the 11111111 to 11111110 transition when the input voltage is 1/2 LSB (20 mV for a 10.24V scale). In most cases, this can be accomplished by having a 1 kΩ pot on pin 5. A resistor of 475Ω can be used as a non-adjustable best approximation from pin 5 to ground.

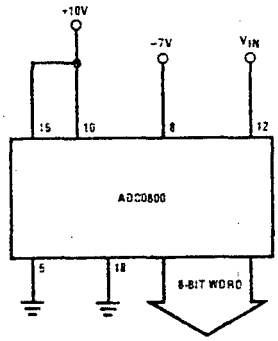
Full-Scale Adjustment: This is the offset voltage required at the top of the R-network (pin 15) to make the 00000001 to 00000000 transition when the input voltage is 1 1/2 LSB from full-scale (60 mV less than full-scale for a 10.24V scale). This voltage is guaranteed to be within 2 LSB for the ADC0800. In most cases, this can be accomplished by having a 1 kΩ pot on pin 15.

Typical Applications

General Connection

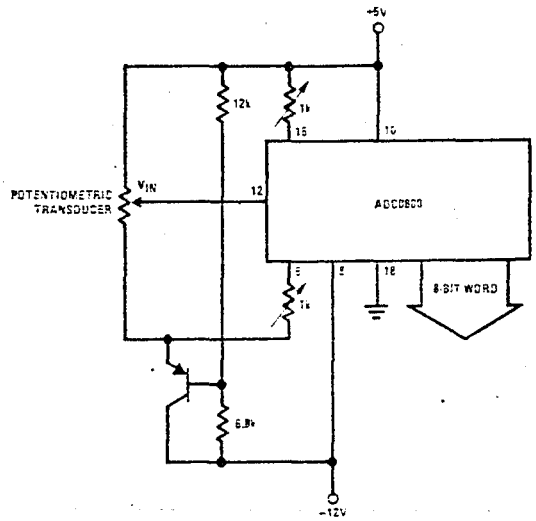


Hi-Voltage CMOS Output Levels



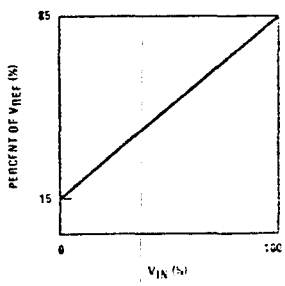
0V to 10V V_{IN} range
0V to 10V output levels

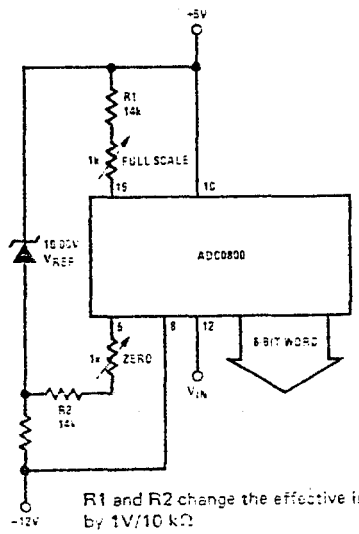
Ratiometric Input Signal with Tracking Reference



Level Shifted Zero and Full-Scale for Transducers

Level Shifted Input Signal Range

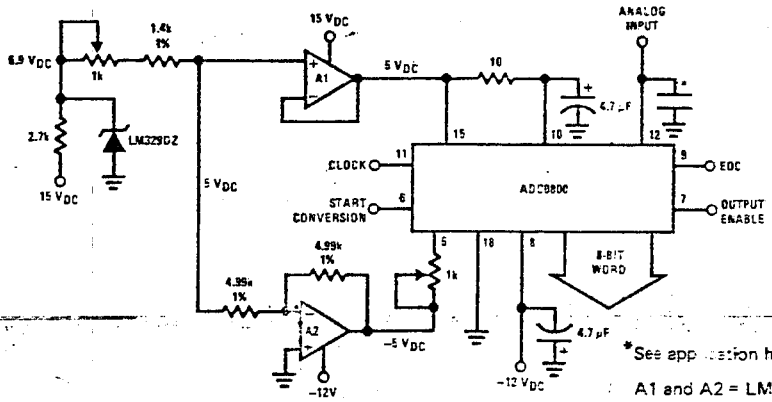




R1 and R2 change the effective input range by 1V/10 kΩ

Typical Applications (Continued)

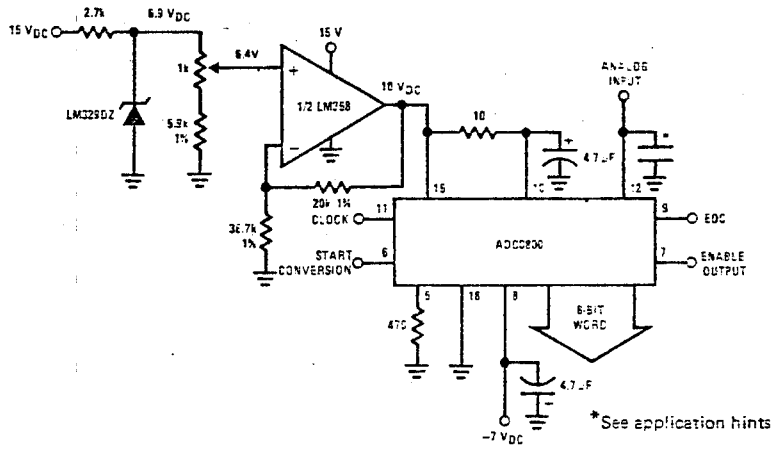
$V_{REF} = 10\ V_{DC}$ With TTL Logic Levels



*See application hints

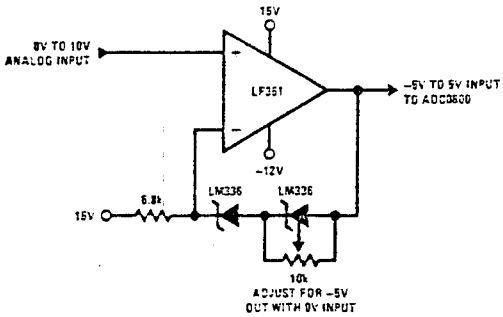
A1 and A2 = LM358N dual op amp

$V_{REF} = 10\ V_{DC}$ With 10V CMOS Logic Levels



*See application hints

Input Level Shifting



- Permits TTL compatible outputs with 0V to 10V input range (0V to −10V input range achieved by reversing polarity of zener diodes and returning the 6.8k resistor to V^-).

MICROPROCESSOR INTERFACE

Figure 3 and the following sample program are included to illustrate both hardware and software requirements to allow output data from the ADC0800 to be loaded into the memory of a microprocessor system. For this example, National's INS8060, SC/MP II, microprocessor has been used.

The sample program, as shown, will start the converter, load the converter's output data into the accumulator, keep track of the number of data bytes entered, complement the data and store this data into sequential memory locations. After 256 bytes have been entered, the control jumps to the user's program where proces-

Typical Applications (Continued)

sing of the data entered will be implemented. A more practical program whereby each data byte entered will be processed before another entry is made can easily be done by jumping back to the user's program at the end of the interrupt routine (where the data is loaded into the accumulator and stored in memory). The end of the user's program should provide a jump back to the INITIALIZE statement to start a new conversion and generate a new data entry.

The following arbitrarily chosen addresses and pointer assignments are used in this example:

Pointer 1 — WORD COUNT (ADDR:0100)
Also used to point to the A/D converter at address 0500 for this example when data is to be entered.

Pointer 2 — ENTERED DATA (ADDR's: 0200→ 02FF)
Data is stored in 2's complement binary form, i.e, 01111111 → +full-scale and 10000000→ — full-scale.

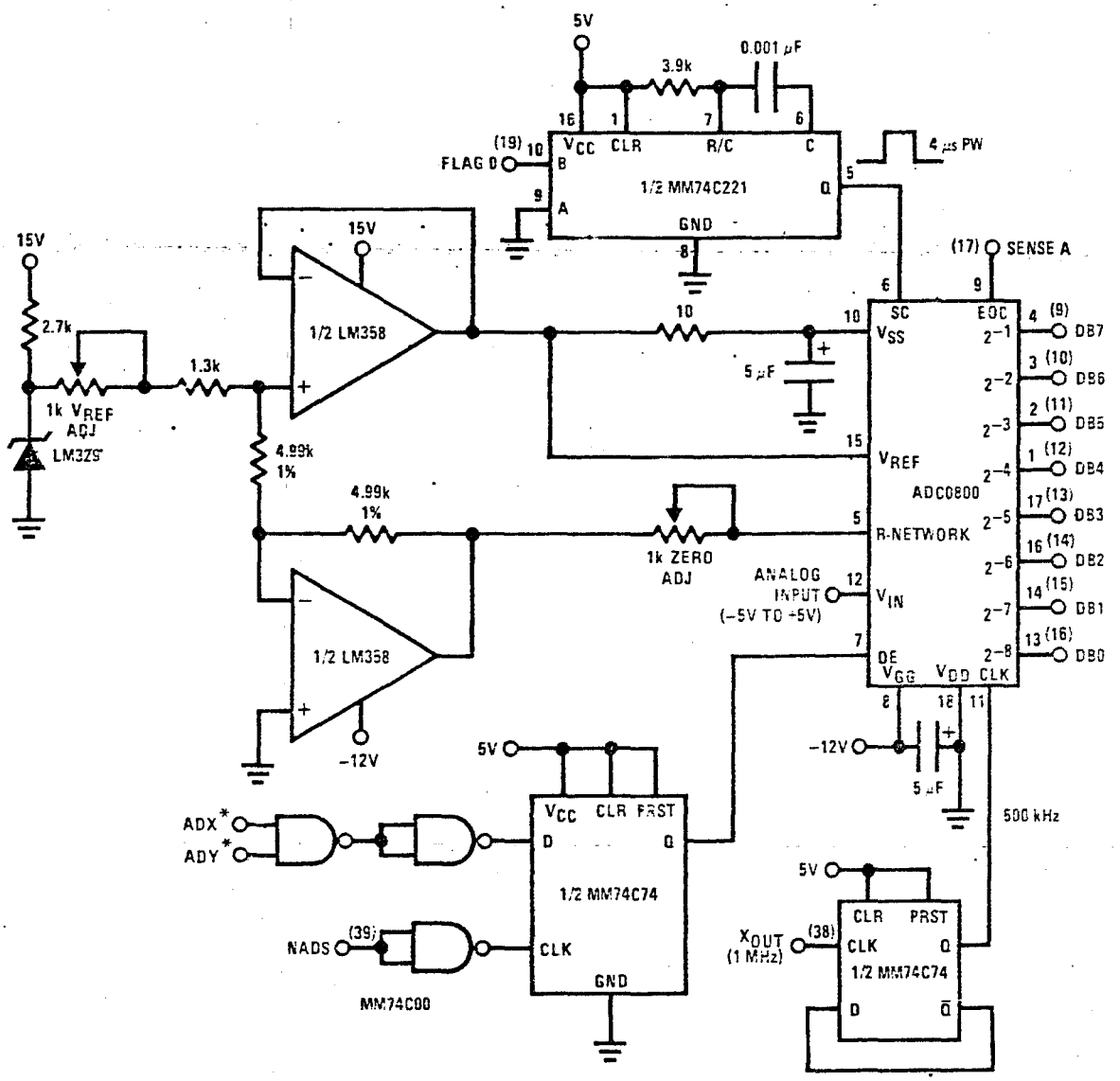
Pointer 3 — LOAD DATA SUBROUTINE (starts at ADDR:0300)
Executed when an EOC signal generates an interrupt request via sense A after an IEN (interrupt enable) instruction.

The address for the converter (0500) is unique for this particular sample program but may not be in a user's system so a different converter address must be used. Note that in *Figure 3* ADX and ADY for the address decode circuitry would be address bits ADB10 and ADB8 (pins 35 and 33 on the SC/MP II package) for converter address 0500.

SAMPLE PROGRAM TO LOAD DATA INTO MEMORY WITH SC/MP II.

```
0001  08      START:      NOP
0002  C4 01                LDIX'01
0004  35                  XPAH 1
0005  C4 00                LDIX'00
0007  31                  XPAL 1      ; P1 = 0100
0008  C4 02                LDIX'02
000A  36                  XPAH 2
000B  C4 00                LDIX'00
000D  C9 00                ST(P1)      ; Zero word count (P1)
000F  32                  XPAL 2      ; P2 = 0200
0010  C4 03                LDIX'03
0012  37                  XPAH 3
0013  08      INITIALIZE: NOP
0014  C4 00                LDIX'00
0016  33                  XPAL 3      ; P3 = 0300
0017  C4 01                LDIX'01
0019  07                  CAS         ; Starts converter via flag 0
001A  C1 00                LD (P1)
001C  F4 FF                XRIX'FF
001E  98 05                JZ DTA IN   ; Test to see if word count is FF,
                                         if so, jump to DTA IN
0020  05                  IEN         ; Enables INTERRUPT
0021  08      LOOP:       NOP
0022  90 FE                JMP LOOP    ; Loop until EOC
0024  08      DTA IN:     NOP
                          .
                          .
                          .           ; User program to process data
                          .
                          .
                          .
   :DATA ENTRY SUBROUTINE
0300  08      DATA IN SR: NOP
0301  A9 00                ILD (P1)    ; Increment word count
0303  C4 05                LDIX'05
0305  35                  XPAH 1      ; P1 will point to converter
0306  C1 00                LD (P1)     ; Converter data loaded into
                                         accumulator
0308  F4 7F                XRIX'7F     ; Put data in 2's complement form
030A  CE 01                ST @ 1(P2)  ; Store data
030C  C4 00                LDIX'00
030E  07                  CAS         ; Resets flag 0
030F  C4 01                LDIX'01
0311  35                  XPAH 1      ; Resets P1 to point at word count
0312  C4 13                LDIX'13
0314  33                  XPAL 3
0315  3F                  XPPC 3      ; Return to INITIALIZE to start a
                                         new conversion
```

Typical Applications (Continued)



- Setting flag 0 (FLG0 = 1) with software, starts conversion (FLG0 must be cleared before another conversion can be initiated)
- With interrupt enabled an EOC will force an interrupt. Interrupt subroutine should load converter data into the accumulator.
- Output data is in complementary offset binary form
- Numbers in parentheses denote pin numbers of SC/MP chip

*ADX and ADY can be any of the address lines but they must be high *only* at the time the converter output data is to be put on the data bus (i.e., the converter must have its own unique address)

FIGURE 3. Interfacing to the SC/MP II Microprocessor

Typical Applications (Continued)

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LED's to display the resulting digital output code as shown in *Figure 4*. Note that the LED drivers invert the digital output of the A/D converter to provide a binary display. A lab DVM can be used if a precision voltage source is not available. After adjusting the zero and full-scale, any number of points can be checked, as desired.

For ease of testing, a 10.24 V_{DC} reference is recommended for the A/D converter. This provides an LSB of 40 mV (10.240/256). To adjust the zero of the A/D, an analog input voltage of 1/2 LSB or 20 mV should be applied and the zero adjust potentiometer should be set to provide a flicker on the LSB LED readout with all the other display LEDs OFF.

To adjust the full-scale adjust potentiometer, an analog input which is 1 1/2 LSB less than the reference (10.240–0.060 or 10.180 V_{DC}) should be applied to the analog input and the full-scale adjusted for a flicker on the LSB LED, but this time with all the other LEDs ON.

A complete circuit for a simple A/D tester is shown in *Figure 5*. Note that the clock input voltage swing and the digital output voltage swings are from 0V to 10.24V. The MM74C901 provides a voltage translation to 5V operation and also the logic inversion so the readout LEDs are in binary.

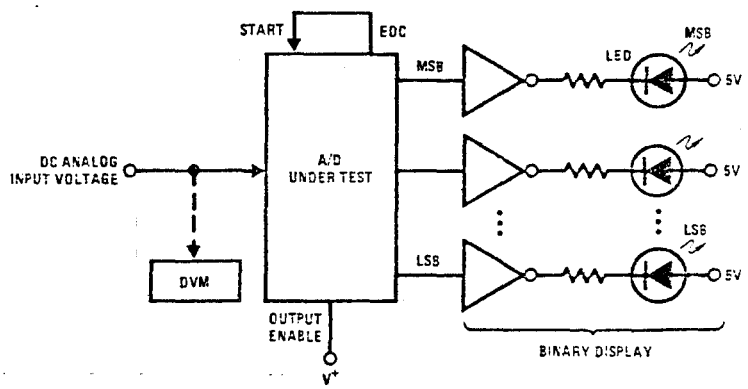


FIGURE 4. Basic A/D Tester

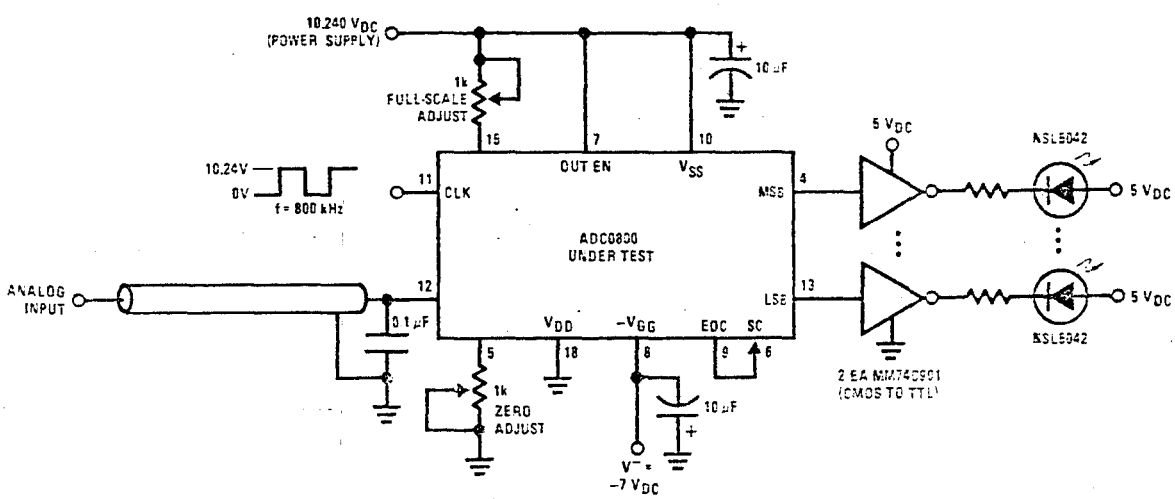


FIGURE 5. Complete Basic Tester Circuit

Typical Applications (Continued)

The digital output LED display can be decoded by dividing the 8 bits into the 4 most significant bits and 4 least significant bits. Table I shows the fractional binary equivalent of these two 8-bit groups. By adding the decoded voltages which are obtained from the column: "Input Voltage Value with a 10.240 V_{REF}" of both the MS and LS groups, the value of the digital display can be determined. For example, for an output LED display of "1011 0110" or "B6" (in hex) the voltage values from the table are 7.04 + 0.24 or 7.260 V_{DC}. These voltage values represent the center values of a perfect A/D converter. The input voltage has to change by ±1/2 LSB (±20 mV), the "quantization uncertainty" of an A/D, to obtain an output digital code change. The effects of this quantization error have to be accounted for in the interpretation of the test results. A plot of this natural error source is shown in *Figure 6* where, for clarity, both the analog input voltage and the error voltage are normalized to LSBs.

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		INPUT VOLTAGE VALUE WITH 10.24 V_{REF}	
		MS GROUP	LS GROUP	MS GROUP	LS GROUP
F	1 1 1 1	15/16	15/256	9.600	0.600
E	1 1 1 0	7/8	7/128	8.960	0.560
D	1 1 0 1	13/16	13/256	8.320	0.520
C	1 1 0 0	3/4	3/64	7.680	0.480
B	1 0 1 1	11/16	11/256	7.040	0.440
A	1 0 1 0	5/8	5/128	6.400	0.400
9	1 0 0 1	9/16	9/256	5.760	0.360
8	1 0 0 0	1/2	1/32	5.120	0.320
7	0 1 1 1	7/16	7/256	4.480	0.280
6	0 1 1 0	3/8	3/128	3.840	0.240
5	0 1 0 1	5/16	5/256	3.200	0.200
4	0 1 0 0	1/4	1/64	2.560	0.160
3	0 0 1 1	3/16	3/256	1.920	0.120
2	0 0 1 0	1/8	1/128	1.280	0.080
1	0 0 0 1	1/16	1/256	0.640	0.040
0	0 0 0 0			0	0

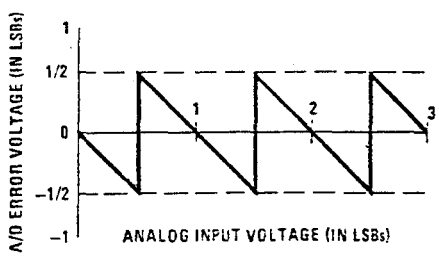


FIGURE 6. Error Plot of a Perfect A/D Showing Effects of Quantization Error

Typical Applications (Continued)

A low speed ramp generator can also be used to sweep the analog input voltage and the LED outputs will provide a binary counting sequence from zero to full-scale.

The techniques described so far are suitable for an engineering evaluation or a quick check on performance. For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be provided as either analog voltages or differences in two digital words.

A basic A/D tester which uses a DAC and provides the error as an analog output voltage is shown in *Figure 7*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to directly readout the difference voltage, "A–C". The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 8* where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

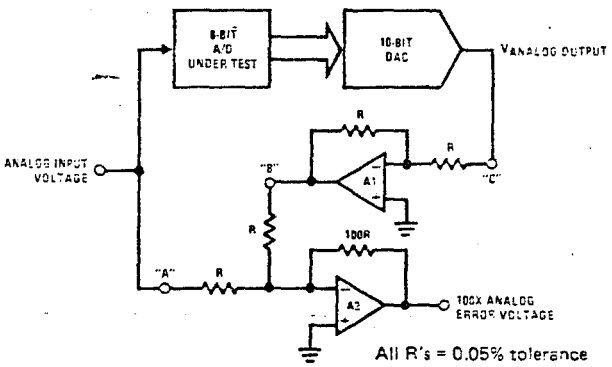


FIGURE 7. A/D Tester with Analog Error Output

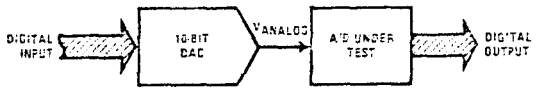
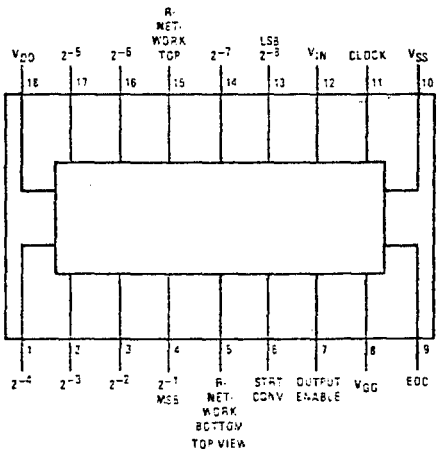


FIGURE 8. Basic "Digital" A/D Tester

Connection Diagram

Dual-In-Line Package



Order Number ADC0800PD (–55°C to +125°C)
or ADC0800PCD (0°C to +70°C)
See NS Package D18A

EK 4 : Sistem programları

```
MULTIPLEXER     EQU  8003h
HATA1           EQU  8004h
HATA2           EQU  8005h
HATA1_2         EQU  8004h
HATA3           EQU  8006h
KeyKod          EQU  8007h
Vtol            EQU  800Ch
Imax            EQU  800Eh
Vout            EQU  800Fh
Vadc            EQU  8000h
Vsend           EQU  8010h
Vread           EQU  8000h
ROLE            EQU  8008h

                ORG  0F00h
VMAXMIN         DB   'max. 24V,min. 0V'
PIMAX           DB   'Imax='
PVOUT           DB   'Vout='
CGR             DB   ' CIKIS GERILIMI '
VOLT            DB   'volt'
HTLGR           DB   '  HATALI GIRDI  '
SPACE           DB   '                '
IVM             DB   'Izin verilen max'
CK5             DB   ' cikis akimi 5 A'
IMAXMIN         DB   'min.100mA,max.5A'
AMPER           DB   'amper'
CKV             DB   ' Cikis Voltaji  '
TLR             DB   '   Toleransi    '
MYUZ            DB   'min. 100mv'
PVTOL           DB   'Vtol='
PROG            DB   'PROGRAMLANABILIR'
GKN             DB   '  GUC  KAYNAGI  '
VVI             DB   'Vout, Vtol, Imax'
VVI2            DB   ' Degerlerini'
VVI3            DB   ' Giriniz '
CKHZ            DB   '  CIKIS HAZIR   '
BTB             DB   'Bir Tusa Basiniz'
LMD1            DB   ' CALISMA LIMITI '
LMD2            DB   '    GECILDI     '
CKL             DB   'Cikis, limitler '
ICD             DB   '    Icinde      '
DecTab1         DB   00h,64h,0C8h
DecTab2         DB   00h,0Ah,14h,1Eh,28h,32h,3Ch,46h,50h,5Ah
KeyTab          DB   22h,36h,26h,16h,11h,35h,25h,15h
KeyTab2         DB   21h,34h,31h,33h,23h,32h,17h
TABLEVout       DB   03h,04h,05h,07h,07h,08h,09h,0Ah,0Bh,
                     0Ch,0Dh,0Eh,10h,11h
v2              DB   11h,13h,14h,15h,16h,17h,18h,19h,1Ah,
                     1Ch,1Ch,1Dh,1Eh
v3              DB   1Fh,21h,21h,22h,23h,25h,26h,26h,27h,
                     28h,2Ah,2Bh,2Bh
v4              DB   2Dh,2Eh,2Fh,30h,30h,31h,32h,34h,35h,
                     35h,37h,38h,39h
```

```
v5              DB    3Ah,3Ah,3Bh,3Dh,3Eh,40h,40h,41h,42h,
                      43h,44h,44h,46h
v6              DB    47h,48h,49h,49h,4Ah,4Ch,4Dh,4Eh,4Eh,
                      4Fh,51h,52h,54h
v7              DB    54h,55h,56h,57h,58h,58h,5Ah,5Ch,5Dh,
                      5Eh,5Eh,5Fh,60h
v77             DB    62h,62h,63h,64h,65h,66h,66h,68h,6Ah,
                      6Ah,6Ch,6Ch,6Eh
v8              DB    6Eh,70h,71h,71h,72h,74h,75h,76h,76h,
                      78h,78h,7Ah,7Bh
v9              DB    7Bh,7Ch,7Dh,7Eh,80h,80h,81h,82h,84h,
                      85h,85h,86h,88h
v10             DB    89h,8Ah,8Ah,8Ch,8Dh,8Eh,8Fh,8Fh,90h,
                      92h,93h,93h,94h
v11             DB    96h,98h,98h,9Ah,9Ah,9Bh,9Ch,9Eh,9Eh,
                      0A0h,0A0h,0A2h,0A2h
v12             DB    0A2h,0A4h,0A6h,0A6h,0A8h,0A8h,0A9h,
                      0ABh,0ACh,0AEh
v13             DB    0AEh,0AEh,0B0h,0B0h,0B2h,0B2h,0B4h,
                      0B4h,0B6h,0B6h
v14             DB    0B8h,0B8h,0BAh,0BAh,0BCh,0BCh,0BEh,
                      0BEh,0C0h,0C2h,0C2h
v15             DB    0C2h,0C4h,0C5h,0C7h,0C7h,0C9h,0C9h,
                      0CBh,0CBh,0CBh
v16             DB    0CDh,0CFh,0D1h,0D1h,0D1h,0D3h,0D3h,
                      0D5h,0D7h,0D7h
v17             DB    0D7h,0D9h,0DBh,0DBh,0DBh,0DDh,0DFh,
                      0DFh,0E1h,0E1h
v18             DB    0E1h,0E3h,0E5h,0E7h,0E7h,0E7h,0E9h,
                      0E9h,0EBh,0EBh
v19             DB    0EBh,0EDh,0EDh,0EFh,0EFh,0F1h,0F1h,
                      0F3h,0F5h,0F5h
v20             DB    0F5h,0F7h,0F7h,0F7h
TABLEImax       DB    03h,07h,0Ch,11h,15h,1Ah,1Eh,23h,28h,
                      2Ah,2Dh,32h,36h
I2              DB    3Bh,40h,44h,49h,4Dh,52h,54h,5Ah,5Fh,
                      64h,66h,6Ah,6Fh
I3              DB    74h,7Ah,7Eh,84h,88h,8Ch,90h,94h,9Ah,
                      9Eh,0A2h,0A8h
I4              DB    0ACh,0B2h,0B6h,0BBh,0C0h,0C5h,0CBh,
                      0CDh,0D1h,0D7h
I5              DB    0DDh,0E1h


ACILIS:         CALL  DISPLAY
                MVI   A,0Fh
                OUT   00h
                MVI   A,01h
                OUT   02h
                LXI   H,PROG
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
```

```
                LXI   H,GKN
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                MVI   A,0Ch
                OUT   01h
                CALL  CNT
                CALL  DELAY2
ACS:            MVI A,01h
                OUT 01h
                CALL CNT
                CALL DELAY1
                LXI   H,VVI
                MVI   B,24h
                MVI   A,0C0h
                CALL  PRINT
                CALL  DELAYD
LPTT:           MVI A,18H
                OUT 01H
                CALL CNT
                CALL DELAYD
                CALL SCAN
                JZ   LPTT
                CALL DELAY
                CALL SCAN
                JZ   LPTT
                CALL Findkeykod
                CALL DISPLAY
                LDA  Keykod
                CPI  31h
                JZ   GetVout
                CPI  33h
                JZ   GetVtol
                CPI  23h
                JZ   Getlmax
                CPI  32h
                JZ   Start
                JMP  LPTT

DELAYD:         LXI   D,0FFFBh
DLYD:           DCX   D
                MOV   A,E
                ORA   D
                JNZ   DLYD
                RET

GETVout:        LXI   H,CGR
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,VMAXMIN
```

```
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                LXI   H,VMAXMIN
                MVI   B,10H
                MVI   A,80H
                CALL  PRINT
                LXI   H,SPACE
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                LXI   H,PVOUT
                MVI   B,05h
                MVI   A,0C0h
                CALL  PRINT
                CALL  GET
                LXI   H,VOLT
                MVI   B,04h
                CALL  PRINTL
                CALL  DELAYM
                CALL  DELAYM
                CALL  DecBin
                STA   Vout
                CPI   0F1h
                JC    ACS
                LXI   H,HTLGR
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                JMP   GetVout

GetImax:        LXI   H,IVM
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,CK5
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                LXI   H,IMAXMIN
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,SPACE
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                LXI   H,PIMAX
```

```
                MVI   B,05h
                MVI   A,0C0h
                CALL  PRINT
                CALL  GET
                LXI   H,AMPER
                MVI   B,05h
                CALL  PRINTL
                CALL  DELAYM
                CALL  DELAYM
                CALL  DecBin
                STA   Imax
                CPI   33h
                JNC   ERROR2
                CPI   01h
                JNC   ACS
                MVI   A,01h
                STA   Imax
                JMP   ACS

Error2:         LXI   H,HTLGR
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                JMP   GetImax


GetVtol:        LXI   H,CKV
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,TLR
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                CALL  DELAYM
                CALL  DELAYM
                LXI   H,SPACE
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,MYUZ
                MVI   B,0Ah
                MVI   A,83h
                CALL  PRINT
                LXI   H,SPACE
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                LXI   H,PVTOL
                MVI   B,05h
```

```
                MVI   A,0C0h
                CALL  PRINT
                CALL  GET
                MVI   B,04h
                LXI   H,VOLT
                CALL  PRINTL
                CALL  DELAYM
                CALL  DELAYM
                CALL  DecBin
                STA   Vtol+01h
                CPI   01h
                JNC   ACS
                MVI   A,01h
                STA   Vtol
                JMP   ACS

DecBin:         MVI   C,01h
                LXI   H,8100h
DLP1:           MOV   A,M
                INX   H
                CPI   17h
                JZ    DLP2
                CPI   32h
                JNZ   DLP1
                MOV   A,L
                DCX   H
                DCX   H
                CPI   01h
                JZ    Error
                CPI   04h
                JNC   Error
                CPI   03h
                JZ    Onlar1
                JMP   Birler2
DLP2:           MVI   C,02h
                MOV   A,L
                CPI   04h
                JNC   Error
                CPI   03h
                JZ    Yuzler
                CPI   02h
                JZ    Onlar
                MOV   A,M
                RET

Yuzler:         LXI   H,8100h
                MOV   A,M
                CPI   03h
                JNC   Error
                LXI   D,DecTab1
                ADD   E
                MOV   E,A
```

```
                XCHG
                MOV   B,M
                XCHG
                INX   H
                MOV   A,M
                LXI   D,DecTab2
                ADD   E
                MOV   E,A
                LDAX  D
                ADD   B
                INX   H
                INX   H
                ADD   M
                RET

Onlar1:         LXI   H,8100h
                MOV   A,M
                CPI   03h
                JNC   ERROR
Onlar:          LXI   H,8100h
                MOV   A,M
                LXI   D,DecTab2
                ADD   E
                MOV   E,A
                MOV   A,L
                ADD   C
                MOV   L,A
                LDAX  D
                ADD   M
                DCR   C
                RNZ
                RLC
                MOV   B,A
                RLC
                RLC
                ADD   B
                RET

Birler2:        LXI   H,8100h
                MOV   A,M
                LXI   D,DecTab2
                ADD   E
                MOV   E,A
                LDAX  D
                RET
ERROR:          LXI   H,HTLGR
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                CALL  DELAYM
                RET
```

```
GET:        LXI  D,8100h
            PUSH D
Get1:       CALL INKEY
            LXI  H,KeyTab
            MVI  B,0Ah
Get2:       CMP  M
            JZ   Rakam
            INX  H
            DCR  B
            JNZ  Get2
            CPI  32h
            JZ   GO
            CPI  17h
            JZ   Dot
            JMP  Get1
Rakam:      MOV  A,L
            SUI  64h
            POP  D
            STAX D
            CALL ASCII
            LXI  H,8002h
            MVI  B,01h
            MVI  A,0C6h
            ADD  E
            INX  D
            PUSH D
            CALL PRINT
            JMP  Get1
Dot:        POP  D
            STAX D
            MVI  A,2Eh
            LXI  H,8000h
            MOV  M,A
            MVI  B,01h
            MVI  A,0C6h
            ADD  E
            INX  D
            PUSH D
            CALL PRINT
            JMP  Get1
GO:         POP  D
            STAX D
            RET

ASCII:      ORI  30h
            STA  8002h
            RET

START:      MVI  A,0Fh
            OUT  00h
            LDA  800Fh
```

```
                CPI   64h
                JNC   OTHER1
                MVI   A,00h
                OUT   02h
                JMP   CONT
OTHER1:         CPI   0B4h
                JNC   OTHER2
                MVI   A,01h
                OUT   02h
                MVI   A,03h
                OUT   02h
                JMP   CONT
OTHER2:         MVI   A,01h
                OUT   02h
                MVI   A,05h
                OUT   02h
CONT:           STA   ROLE
                LXI   H,0000h
                SHLD  HATA1_2
                CALL  SETImax
                CALL  SETVtol
                CALL  SETVout
                LXI   H,CKHZ
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,BTB
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
AGN:            CALL  SCAN
                JZ    AGN
                CALL  DELAY
                CALL  SCAN
                JZ    AGN
                LXI   H,CKL
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,ICD
                MVI   B,10h
                MVI   A,0C0h
                LDA   ROLE
                ORI   08h
                OUT   02h
SLP1:           CALL  SENDVout
SLP2:           CALL  DELAYD
                XRA   A
                STA   MULTIPLEXER
                CALL  READOUT
                LXI   H,Vtol
                LDA   Vadc
                CMP   M
                JNC   OUTTOL
```

```
                INX   H
                CMP   M
                JC    OUTTOL
                XRA   A
                STA   HATA1
                MVI   A,02h
                STA   MULTIPLEXER
                CALL  READOUT
                LXI   H,Imax
                LDA   Vadc
                CMP   M
                JC    KCImax
                LXI   H,HATA2
                INR   M
                MVI   A,03h
                CMP   M
                JNC   SLP1
EXIT:           MVI   A,01h
                OUT   02h
                LXI   H,LMD1
                MVI   B,10h
                MVI   A,80h
                CALL  PRINT
                LXI   H,LMD2
                MVI   B,10h
                MVI   A,0C0h
                CALL  PRINT
                RET
KCImax:         XRA   A
                STA   HATA2
                JMP   SLP2
OUTTOL:         LXI   H,HATA1
                INR   M
                MVI   A,0Ah
                CMP   M
                JC    EXIT
                LDA   Vout
                LXI   H,Vadc
                SUB   M
                JNC   PZT
                CMA
                INR   A
PZT:            CPI   04h
                JC    ADJ
                LXI   H,HATA3
                INR   M
                MVI   A,02h
                CMP   M
                JNC   SLP2
ADJ:            XRA   A
                STA   HATA3
                LXI   H,Vout
                LDA   Vadc
                CMP   M
```

```
                JZ    SLP2
                JC    BUYUK
                INX   H
                DCR   M
                JMP   SLP1
BUYUK:          INX   H
                INR   M
                JMP   SLP1

SETVout:        CALL  SETVread
                XRA   A
                STA   Vsend
                STA   MULTIPLEXER
SVLPT:          CALL  SENDVout
                CALL  DELAYM1
                CALL  READOUT
                LXI   H,Vout
                CMP   M
                JZ    ESIT
                JC    BUYUK2
                INX   H
                DCR   M
                JMP   SVLPT
BUYUK2:         INX   H
                INR   M
                JMP   SVLPT
ESIT:           RET

DELAYM1:        LXI   D,0F0Fh
DLYM1:          DCX   D
                MOV   A,E
                ORA   D
                JNZ   DLYM1
                RET

SETVread:       LXI   H,TABLEVout
                LDA   Vout
                MOV   C,A
                XRA   A
                MOV   B,A
                DAD   B
                MOV   A,M
                STA   Vout
                RET

SETImax:        LXI   H,TABLEImax
                LDA   Imax
                MOV   C,A
                XRA   A
                MOV   B,A
                DAD   B
```

```
                MOV   A,M
                STA   Imax
                RET

SETVtol:        LXI   D,Vout
                LXI   H,Vtol+01h
                LDAX  D
                ADD   M
                LXI   H,TABLEVout
                MOV   C,A
                XRA   A
                MOV   B,A
                DAD   B
                MOV   A,M
                STA   Vtol
                LDAX  D
                LXI   H,Vtol+01h
                SUB   M
                LXI   H,TABLEVout
                MOV   C,A
                XRA   A
                MOV   B,A
                DAD   B
                MOV   A,M
                STA   Vtol+01h
                RET

SENDVout:       LXI   H,Vsend
                MOV   A,M
                OUT   20h
                OUT   21h
                RET

READOUT:        MVI   A,0CEh
                OUT   10h
                MVI   A,14h
                OUT   14h
                MVI   A,40h
                OUT   15h
                MVI   A,0FH
                OUT   00H
                MVI   A,00h
                OUT   03h
                LDA   MULTIPLEXER
                OUT   13h
                MVI   A,01h
                OUT   03H
                MVI   A,00h
                OUT   03h
                CALL  DLY260
                IN    30h
```

```
                STA   Vread
                RET

DLY260:         LXI   D,001Eh
DL:             DCX   D
                MOV   A,E
                ORA   D
                JNZ   DL
                RET

DISPLAY:        MVI   A,0Fh
                OUT   00h
                MVI   A,01h
                OUT   01h
                CALL  CNT
                CALL  DELAY1
                MVI   A,02h
                OUT   01h
                CALL  CNT
                CALL  DELAY1
                MVI   A,38h
                OUT   01h
                CALL  CNT
                CALL  DELAY2
                MVI   A,06h
                OUT   01h
                CALL  CNT
                CALL  DELAY2
                MVI   A,0Eh
                OUT   01h
                CALL  CNT
                CALL  DELAY2
                RET

CNT:            MVI   A,10h
                OUT   03h
                MVI   A,00h
                OUT   03h
                RET

DELAY1:         LXI   D,00E1h
DLY2:           DCX   D
                MOV   A,E
                ORA   D
                JNZ   DLY2
                RET

DELAY2:         LXI   D,0006h
DLY3:           DCX   D
                MOV   A,E
                ORA   D
```

```
                JNZ   DLY3
                RET

PRINT:          OUT   01h
                CALL  CNT
                CALL  DELAY2
PRINTL:         MOV   A,M
                OUT   01h
                CALL  CNTD
                INX   H
                DCR   B
                JNZ   PRINTL
                RET

CNTD:           MVI   A,14h
                OUT   03h
                MVI   A,04h
                OUT   03h
                CALL  DELAY2
                RET

INKEY:          CALL  SCAN
                JNZ   INKEY
LOOP:           CALL  SCAN
                JZ    LOOP
                CALL  DELAY
                CALL  SCAN
                JZ    LOOP
Findkeykod:     MVI   B,00h
LOOP2:          INR   B
                RAR
                JC    LOOP2
                MOV   A,C
                RLC
                RLC
                RLC
                RLC
                ORA   B
                STA   Keykod
                RET

SCAN:           MVI   C,01h
                MVI   A,0Eh
                OUT   10h
                MVI   A,30h
                OUT   13h
                IN    11h
                CPI   0FFh
                RNZ
                INR   C
```

```
                MVI   A,28h
                OUT   13h
                IN    11h
                CPI   OFFh
                RNZ
                INR   C
                MVI   A,18h
                OUT   13h
                IN    11h
                CPI   OFFh
                RET

DELAY:          LXI   D,1568h
DLYDLY:         DCX   D
                MOV   A,D
                ORA   E
                JNZ   DLYDLY
                RET

DELAYM:         LXI   D,OFFFFh
DLYM:           DCX   D
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                NOP
                MOV   A,D
                ORA   E
                JNZ   DLYM
                RET
                END
```