MİKROİŞLEMCİ KONTROLLU AĞIRLIK ÖLÇME SİSTEMİ

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Olarak Hazırlanmıştır.

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Hakan Tora'nın YÜKSEK LİSANS tezi olarak hazırladığı "MİKROİŞLEMCİ KONTROLLU AĞIRLIK ÖLÇME SİSTEMİ" başlıklı bu çalışma, jürimizce lisansüstü yönetmeliğinin ilgili maddeleri uyarınca değerlendirilerek kabul edilmiştir.

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İÇİNDEKİLER

ÖZET

Ağırlık ölçme sisteminde , 8085 mikroişlemcisi ve yük hücresi kullanılmıştır. Ölçme yük hücresinden gelen elektriksel sinyalin (Bu sinyal uygulanan ağırlıkla orantılıdır) instrumantasyon kuvvetlendiricisinde yükseltilmesiyle yapılmıştır. Yükseltecin kazancı aynı zamanda ölçekleme işlemini de yapmaktadır. Daha sonra yükselteç çıkışı 4½ dijitlik bir DVM'den geçirilerek ağırlık bilgisi sayısal olarak mikroişlemciye aktarılmaktadır. Uygun yazılımlarla bu bilgi 7-parçalı göstergelerde ton olarak gözlenmektedir.

İlgili elektronik devrede bir adet 8085 mikroişlemcisi, iki adet 8155 PIO, bir adet 2764 (8Kx8) EPROM, bir adet 6264 (6264) RAM, bir adet 8279 Programlanabilir Tus/Gösterge Arabirimi, bir adet 7135 DVM (4½) ve bir adet INA101 Instrumentation Amlifier entegreleri kullanılmıştır. Bunlara ek olarak iki adet 74LS139 decoder, bir adet 74LS138 decoder, bir adet 74LS373 Latch entegreleri ve altı adet 7-parçalı gösterge de bulunmaktadır.

SUMMARY

In a weight measuring system, a load cell and microprocessor 8085 was used. The signal obtained from the load cell was connected to the instrumentation amplifier. The output from the Instrumentation Amplifier INA101 was transferred to the 4½ digits DVM (BCD outputed ADC). Then the digital data was processed with 8-bit microprocessor. By means of a convenient software, the weighing result was observed on the 7-segment display.

The system contains a 8085 CPU, two 8155 PIO, one EPROM (2764), one RAM (6264), a keyboard/display interface (8279), 4½ digit DVM (7135) and one instrumentation amplifier (INA101). In addition, three decoders (74LS138, 74LS139), one latch and six seven segment display.

TANIMLAR ve KISALTMALAR

ADC	: Analog sayısal çevirici
Bit	: İkilik sayı sisteminde 0 ve 1 olabilen sayı basamağı
Byte	: 8 bitten oluşan birim
Clock	: Periyodik kare dalga sinyali
Counter	: Sayıcı
CPU	: Merkezi işlem birimi
Data	: Veri
Decoder	: Çözücü
DVM	: Dijital voltmetre
EPROM	: Silinebilen programlanabilen ve sadece okunabilen bellek
Hardware	: Donanım
Interrupt	: Kesme
Keyboard	: Tuş takımı
Latch	: Tutucu
Load Cell	: Yük hücresi
Memory	: Bellek
Port	: Mikroişlemcinin dış dünya ile haberleşmesini sağlayan birim
RAM	: Rastgele erişilebilen bellek
Register	: Kütük
Software	: Yazılım
Strain	: Malzemedeki deformasyon
Stres	: Malzemeye uygulanan kuvvet
Transducer	: Dönüştürücü
7-segment display	: 7-parçalı gösterge
xxxxH	: 16'lık sayı sisteminde sayılar

ŞEKİLLER DİZİNİ

TEŞEKKÜR

Bu çalışmayı bana veren ve araştırmalarıma gerek fikir gerekse kaynak yönünden yardımcı olan Sayın Hocam Doç.Dr.Hamdi Atmaca'ya teşekkür ederim.

Ayrıca tez süresince her konuda bana yardımcı olan değerli arkadaşım Arş.Gör.Rıfat Edizkan'a, yazım ve şekil çizimi konularında yardımcı olan arkadaşım Arş.Gör.O.Nuri Çelik'e çok çok teşekkür ederim.

Tezin ilerlemesinde büyük katkıları olan değerli arkadaşlarım Elektronik Mühendisi A.Reşit Kuldemir'e ve Elektronik Mühendisi Mutlu Özkır'a ayrı ayrı teşekkür ederim.

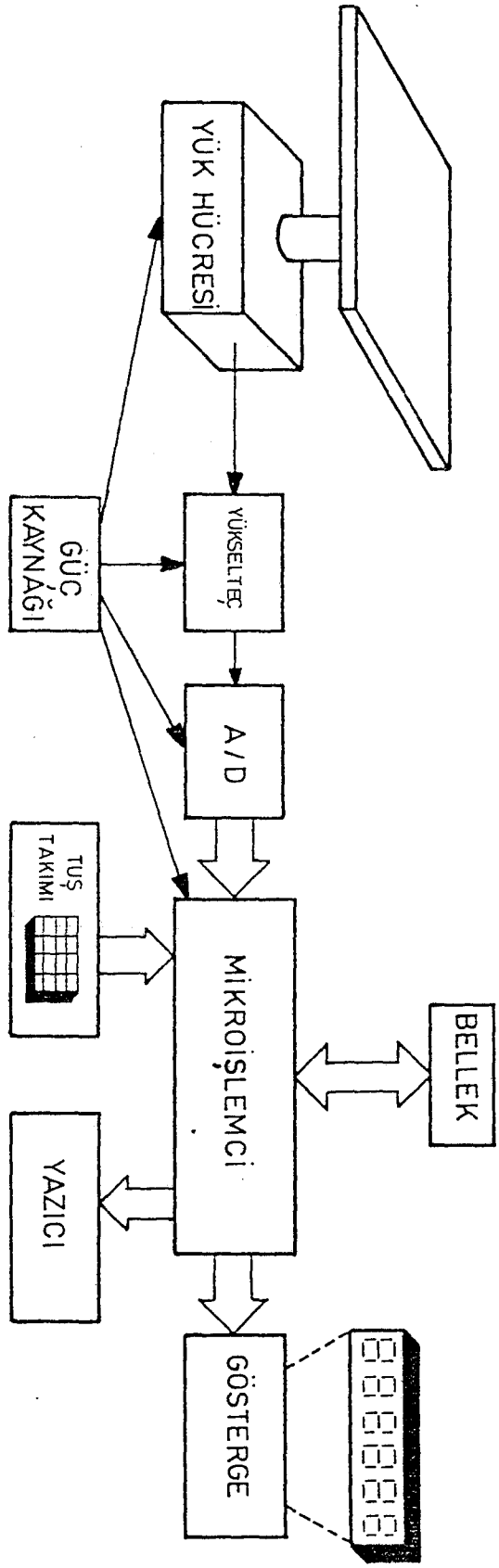
1. GİRİŞ

Bilindiği gibi artık mekanik ve analog bir çok endüstriyel alanda kullanılan sistemler yerlerini elektronik devrelere bırakmışlardır. Ancak bu değişimin olabilmesi için fiziksel büyüklük olarak nitelendirilen basınç, sıcaklık, ağırlık, kuvvet gibi büyüklüklerin elektriksel işaretlere çevrilmesi gerekmektedir. Teknolojinin gelişimiyle birlikte ortaya çıkan dönüştürücüler sayesinde gerçek hayattaki bu büyüklükler elektronik devrelerin anlayacağı dile çevrilebilmiştir.

Bu tez çalışmasında da Yük Hücresi denilen dönüştürücülerden gelen elektriksel sinyaller bir A/D yardımıyla mikroişlemciye alınıp, bu sinyaller uygun şekilde işlenerek bir elektronik kantar yapılmıştır. Cihaz ağırlık ölçmenin yanında ayrıca tarih ve aracın plakasının girilmesine de imkan vermektedir. Ayrıca istendiği anda tarih, plaka ve ağırlık bilgileri bir yazıcı aracılığıyla kağıda aktarılabilmektedir. Tabi ki böyle bir cihazın mekaniklerine göre bir çok avantajı olacaktır. Bunları şu şekilde sıralamak mümkündür:

a) Okuma hatası yok denecek kadar azdır.
b) Bakımı, onarımı ve ayarı kolaydır.
c) Hızlı ölçüm yapabilmektedir.
d) Yazıcı bağlanabildiği için istenilen bilgiler kağıt üzerine yazdırılmaktadır.
e) Ölçme platformu ve ölçme cihazı ayrı olduğundan birbirlerinden uzak yerlere konulabilmektedir.
f) Kullanıcı ile diyaloğu kolaydır.

Şekil 1.1'de gerçekleştirilen elektronik kantarın blok diyagramı gösterilmektedir.



Şekil 1.1 Elektronik Kantarın Blok Diyagramı

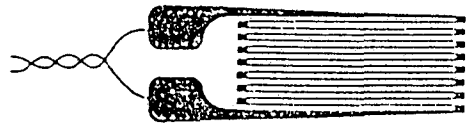
2. DÖNÜŞTÜRÜCÜLER (Transducers)

Dönüştürücüler farklı sistemler arasında enerji aktarımı sağlayan cihazlar olarak tanımlanabilir. Sıcaklık, mesafe, kuvvet, ağırlık, basınç gibi fiziksel büyüklüklerin analog algılayıcıları sayesinde yeni ölçme ve uygulama alanları doğmuştur. Bu tez çalışmasında da Yük Hücresi (Load Cell) kullanılarak ağırlık ölçmeye çalışılmıştır. Yük hücresi çıkışında, üzerine uygulanan ağırlıkla orantılı olarak milivoltlar seviyesinde dc gerilim veren bir dönüştürücüdür. Strain Gage denilen malzemelerden oluşturulmuştur.

2.1 Strain Gage

Strain gage uygulanan kuvvetin yönüne göre boyunun uzaması veye kısalması sonucunda küçük miktarlarda direnç değişimi gösteren iletken bir teldir. Boydaki değişim çok küçüktür.

Şekil 2-1'de bir strain gage'in yapısı gösterilmiştir. Çekme yönünde bir kuvvete maruz kalan strain gage'in direnci artar. Çünkü normal boyunda bir artış olur. Sıkıştırma yönündeki bir kuvvet de strain gage'in boyunu azaltacağından direncinde bir düşme olur. İşte bu direnç değişimi özelliğinden yararlanılarak bu malzemelerden yük hücreleri yapılıp ağırlık ölçümlerinin elektronik olarak yapılması sağlanmıştır.



Şekil 2.1 Strain gage'in yapısı

Strain gage'lerin bazı parametreleri vardır. İmalatçılar tarafından zorlanmaya maruz kalınmadığı zamanki gage'in R direnci verilir. $\triangle R$ değişimi bir kez ölçüldüğünde $\triangle R/R$ oranı hesaplanır. Yine imalatçılar tarafından her gage için

belirlenmiş olan gage faktörü (GF) de verilir. Gage faktörü, bir gage'in direncindeki değişim yüzdesinin boyundaki değişim yüzdesine oranı olarak tanımlanır. Yani $\Delta R/R$ oranı GF'ye bölünürse sonuç $\Delta L/L$ olur. Eğer GF'si 2 olan 120 Ω'luk bir strain gage gerilme yönündeki bir kuvvet nedeniyle 0.001 Ω'luk bir R değişimi göstermiş ise boyundaki değişim yüzdesi;

$$\frac{\Delta L}{L} = \frac{\Delta R/R}{GF} = \frac{0.001/120}{2} = 4.1\ \mu inc/inc$$

olarak bulunur. $\Delta L/L$ oranına birim strain de denir. Burada bazı tanımların verilmesine gerek vardır:

Birim alana uygulanan kuvvet miktarına "stres" denir. Stres'den dolayı bir malzemedeki deformasyona da "strain" denir ki bu da $\Delta L/L$'dir.

Bir strain gage'deki R direnç değişimi bir kaç miliohm gibi küçük bir değere sahiptir. Bunun ölçülebilmesi için öncelikle direnç değişimi akım veya gerilime çevrilmelidir. Dirençteki küçük bir değişim çok küçük bir gerilim değişimine sebeb olacaktır. Örneğin 120 Ω'luk bir strain gage'den 5mA'lik bir akım geçsin. Bu durumda gage'in uçlarındaki gerilim 0.6 V olur. Eğer direnç 1 mΩ kadar değişirse 5 μV'luk bir gerilim değişimi oluşur. Bu değişimi bir voltmetre ile gözleyebilmek için uygun bir katsayıyla çarparak yükseltmek gerekir. Örneğin 1000 katsayısıyla çarpıldığında değişim 5mV olur. Fakat diğer taraftan da 0.6V 600V'a yükselir. Takdir edileceği gibi 600V'luk bir sinyal içinden 5mV'u ayırtetmek oldukça güçtür. Bundan dolayı sadece direnç değişiminin sebep olduğu gerilim farkını yükselten bir devreye ihtiyaç vardır. Bu problem de basit bir direnç köprü devresiyle halledilmektedir.

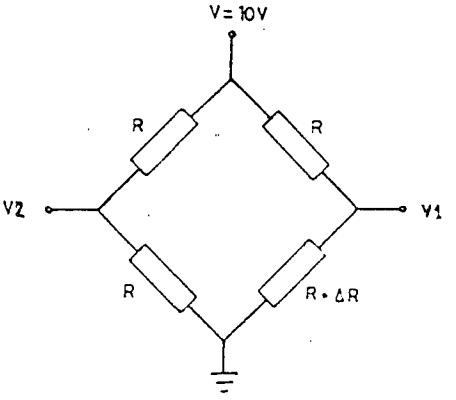
Şekil 2-2'de gösterildiği gibi strain gage direnç köprü devresinin bir koluna yerleştirilir. Devredeki R direncinin değeri herhangi bir kuvvete maruz kalınmadığı zamanki

gage'nin direncidir.

V1=V2=V/2 olduğunda V1-V2=0 olacaktır. Bu şartlar altında köprü dengededir denir. Eğer strain gage sıkıştırılırsa R değeri ΔR kadar azalacaktır. Bu durumda gerilim farkı,

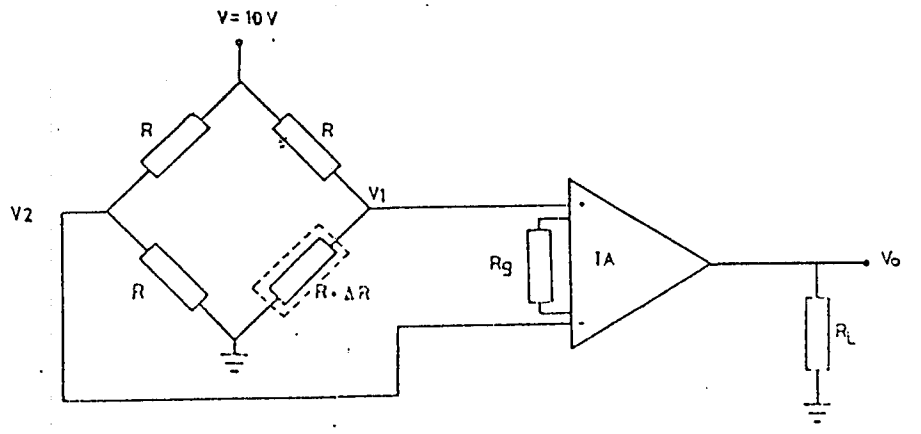
$$V1-V2=E(\Delta R)/4R \qquad (2.1)$$

olarak bulunur. Örneğin R=0.001Ω, R=120Ω, V=10V ise V1-V2 farkı 22μV olur. Görüldüğü gibi bu fark çok küçük bir değerdir. Bu sinyali harici gürültülerden koruyarak yükseltebilmek ancak bir instrumantasyon kuvvetlendirici kullanılarak yapılabilir.



Şekil 2.2 Direnç köprü devresi

Şekil 2.3'de direnç köprü devresinin instrumantasyon kuvvetlendiriciye nasıl bağlandığı gösterilmiştir. Kuvvetlendiricinin kazancı dışardan bağlanan bir Rg direnci ile istenilen değere ayarlanabilir. Eğer kazancı 1000 yapacak şekilde Rg seçilirse yukardaki örnekte 22μV'luk gerilim farkı kuvvetlendiricinin çıkışında 22mV'a yükseltilmiş olur.



Şekil 2.3 Direnç köprü ve Kuvvetlendirici devresi

Sonuç olarak strain gage'ler kullanılarak basınç, kuvvet ve ağırlık büyüklüklerini ölçmek mümkün olmaktadır. İşte strain gage'lerin bu özelliğinden yararlanarak yapılan yük hücreleri sayesinde ağırlıklar elektriksel sinyallere çevrilerek uygun sinyal işleme devrelerine sokulup çok hassas çalışan elektronik kantarlar yapılmaktadır.

3. INSTRUMANTASYON KUVVETLENDİRİCİ

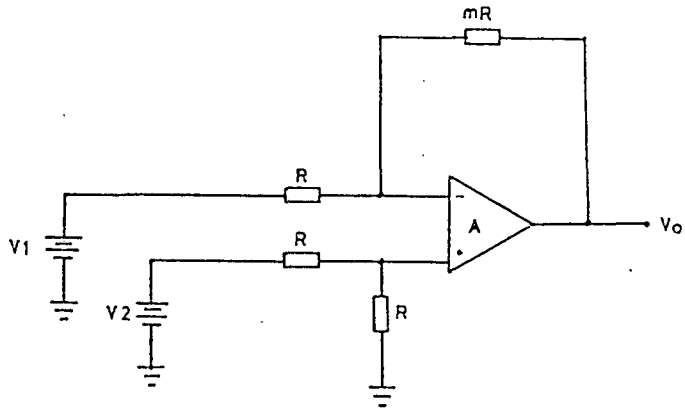
Ölçme ve kontrol sistemlerinde en çok kullanılan kuvvetlendiriciler instrumantasyon kuvvetlendiricilerdir. Bu yükselteçler sadece giriş sinyalleri arasındaki farkı yükseltirler. Giriş empedansları oldukça yüksektir. Dışardan bağlanan bir dirençle kararlı yüksek kazançlar elde edilir. Ortak mod azaltma oranları oldukça yüksektir. Instrumantasyon yükselteçlerini tek bir entegre içinde elde etmek mümkün olabildiği gibi bir kaç işlemsel yükselteç ve dirençlerle de yapmak mümkündür. Ancak aynı verimlilik ve duyarlılık elde edilemez. Instrumantasyon kuvvetlendiricilerin en basit şekli bir fark yükseltecidir.

3.1 Fark Yükselteci

Fark yükselteçleri girişlerindeki gerilimlerin farkını alıp istenilen bir kazançla çıkışa yansıtan devrelerdir. Şekil 3.1'de gösterilen fark yükseltecinin çıkışı şu şekilde yazılabilir:

$$Vo=m(V2-V1) \qquad (3.1)$$

Görüldüğü gibi Vo çıkış gerilimi yükseltecin + ve - girişlerine uygulanan gerilimlerin farkıyla orantılıdır. "m" çarpanı ise fark kazancıdır ki bu da direnç oranları ile ayarlanır.



Şekil 3.1 Fark Yükselteci

Böyle bir devrede CMRR (ortak mod azaltma oranı)'ın iyi olabilmesi için dirençlerin çok hassas ve de %1'lik olması gerekmektedir. Ortak mod azaltma oranı (CMRR); bir kuvvetlendiricinin ortak mod ve fark kazançlarının oranı şeklinde tanımlanır:

$$CMRR = \frac{Adm}{Acm} \qquad (3.2)$$

İdeal CMRR sonsuz olarak kabul edilir. Bir fark kuvvetlendiricisinin fark girişlerini yükseltip ortak mod sinyallerini yok etmesi o kuvvetlendiricinin CMRR'ı ile belirlenir. Fark yükselteçlerinin bir dezavantajı giriş empedanslarının yeteri kadar büyük olmamasıdır.

Ortak mod etkisini azaltmak, giriş empedansını arttırabilmek ve değişken yüksek kazançlar elde edebilmek için instrumantasyon kuvvetlendiricileri kullanılır.

3.2 Instrumantasyon Kuvvetlendiricinin Kazancı

Instrumantasyon kuvvetlendiriciler sayesinde µV ve mV seviyesindeki sinyaller istenmeyen gürültü sinyallerinden korunarak yükseltilebilir. Şekil 3.2'de bir instrumantasyon kuvvetlendiricisi görülmektedir. Bu devrenin gerilim kazancı şu şekilde hesaplanabilir:

A noktasındaki VA gerilimi,

$$VA = \frac{R}{aR} (V1 - V2) + V1 \qquad (3.3)$$

Bnoktasındaki VB gerilimi,

$$VB = \frac{R}{aR} (V2 - V1) + V2 \qquad (3.4)$$

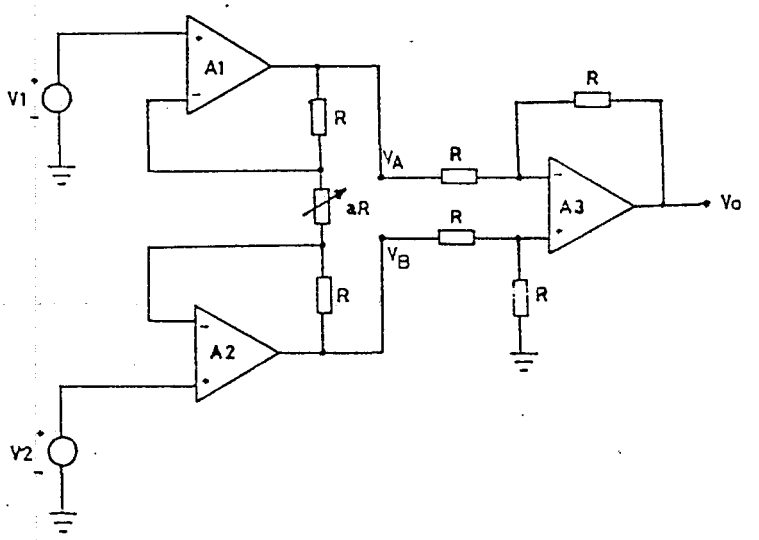
olarak yazılabilir. VB ve VA fark yükseltecinin girişlerine uygulanmaktadır. O halde,

$$Vo=VB-VA=\left(1+\frac{2}{a}\right)(V2-V1) \qquad (3.5)$$

$$\frac{Vo}{V2-V1}=\left(1+\frac{2}{a}\right) \qquad (3.6)$$

olarak gerilim kazancı hasaplanır.

Kazanç denkleminden de görüldüğü gibi devrede bulunan R ve aR değerleri ile kazanç ayarı yapmak mümkündür. Bu kuvvetlendiricilerin giriş empedansı çok yüksek olduğu için sinyalin zayıflaması da önlenmektedir.



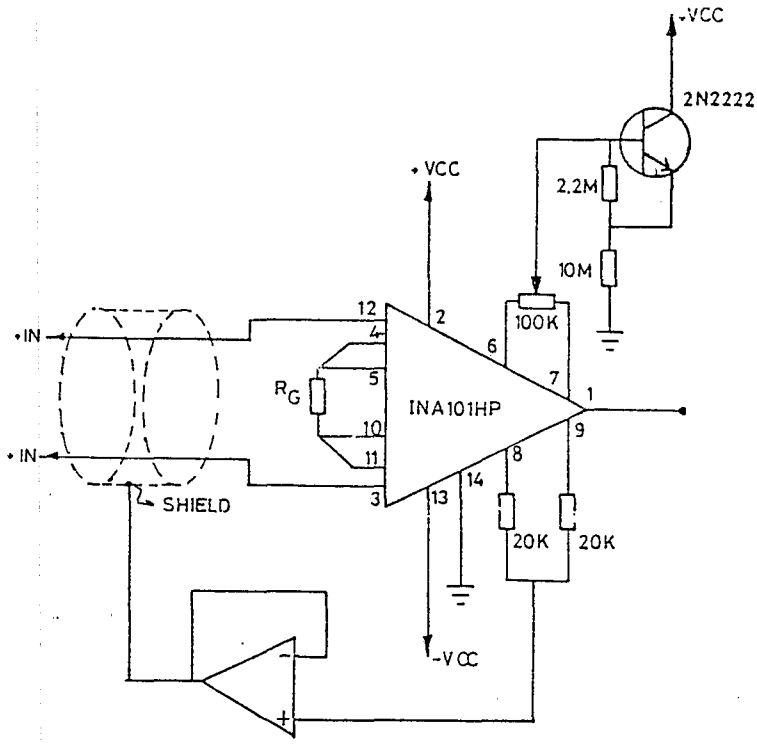
Şekil 3.2 Instrumantasyon Kuvvetlendiricisi

3.3 INA101 Instrumantasyon Kuvvetlendiricisi

Şekil 3.3'de gösterilen devre tezde kullanılmıştır. 5 ve 10 nolu bacaklar arasına bağlanan Rg direnci ile istenilen kazanç ayarlanabilmektedir. 2 ve 3 nolu bacaklara bağlanmış olan 100K'lık potansiyometre ile çıkış ofset gerilimi ayarlanabilmektedir. Devrenin gerilim kazancı,

$$G = 1 + \frac{40K}{Rg} \qquad (3.7)$$

formülüyle hesaplanmaktadır.(BURR-BROWN Data Book,Sayfa;2-12)



Şekil 3.3 INA101 Instrumantasyon Yükselteci

Kuvvetlendiricinin 8 ve 9 nolu bacakları entegre içerisindeki fark yükselteci katının girişleridir. Bu nedenle dışardan gürültü almaması için bunlar bir gerilim tampon devresiyle shield'lanmıştır. Böylece dışardaki elektromanyetik dalgaların yaratacağı etkilerden sistem korunmuştur.

3.4 Alçak Geçiren Filtre

Tasarlanan sistemde ikinci dereceden bir butterworth alçak geçiren filtre kullanılmıştır. Kesim frekansı 2Hz ve kazancı "1" olacak şekilde elemanlar seçilmiştir. Filtre devresi Şekil 4.2'de görüldüğü gibi kuvvetlendirici ile DVM devreleri arasına yerleştirilmiştir. Böylece trafo veya load cell'den kaynaklanan bir takım gürültü bileşenleri filtre devresinde süzülerek mikroişlemciye ulaşmaktadır. Alçak geçiren filtrenin kesim frekansı şu formülle hesaplanmaktadır:

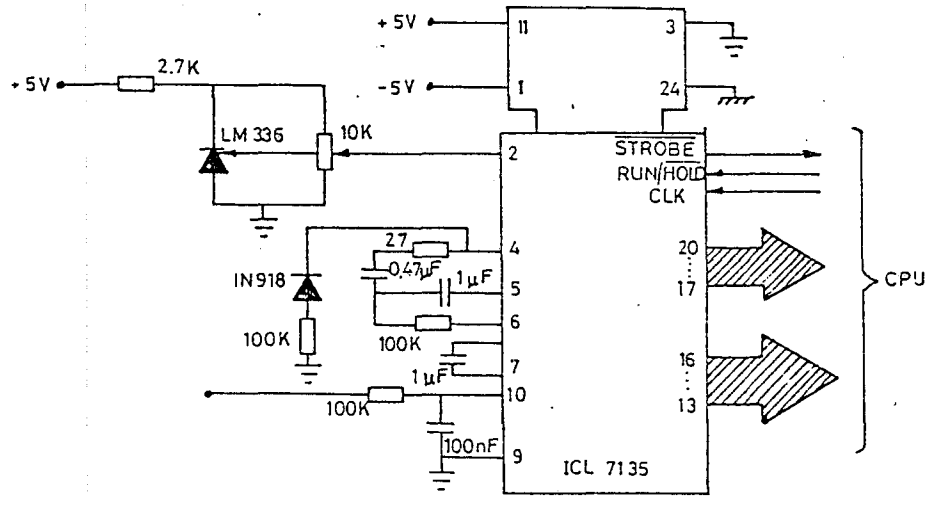
$$fc = \frac{1}{2\pi(R1R2C3C4)^{1/2}} \qquad (3.8)$$

4. ANALOG-SAYISAL ÇEVİRİCİ DEVRESİ

Analog işaretlerin bir mikroişlemci tarafından işlenebilmesi için öncelikle sayısal işaretlere çevrilmesi gerekir. Bu işlem de analog-sayısal çevirici entegre devreleri sayesinde yapılmaktadır. Tez çalışmasında yapılan elektronik kantar devresinde de INTERSIL'in 7135 A/D entegresi kullanılmıştır. Bu çevirici dual-slope tekniğini kullanan 4½ dijitlik bir dijital voltmetredir (DVM). Bu DVM'in tam bir A/D gibi çalışabilmesi için sadece dışardan bir gerilim referansı, bir kaç direnç ve kapasitör ilave etmek yeterlidir.

4.1 Sistemde Kullanılan Devre

Şekil 4.1'de yapılan ADC devresi gösterilmiştir. Devrenin ihtiyacı olan referans voltajı LM336 2.5V hassas referans entegresi ile sağlanmıştır. Uçlarına paralel olarak bağlanan 10KΩ'luk bir potansiyometre ile referans voltajı 1V'a ayarlanmıştır. Devre 125KHz'lik saat frekansı ile dönüştürme işlemini yapmaktadır.(INTERSIL, Sayfa: 3-74)



Şekil 4-1 DVM Devresi

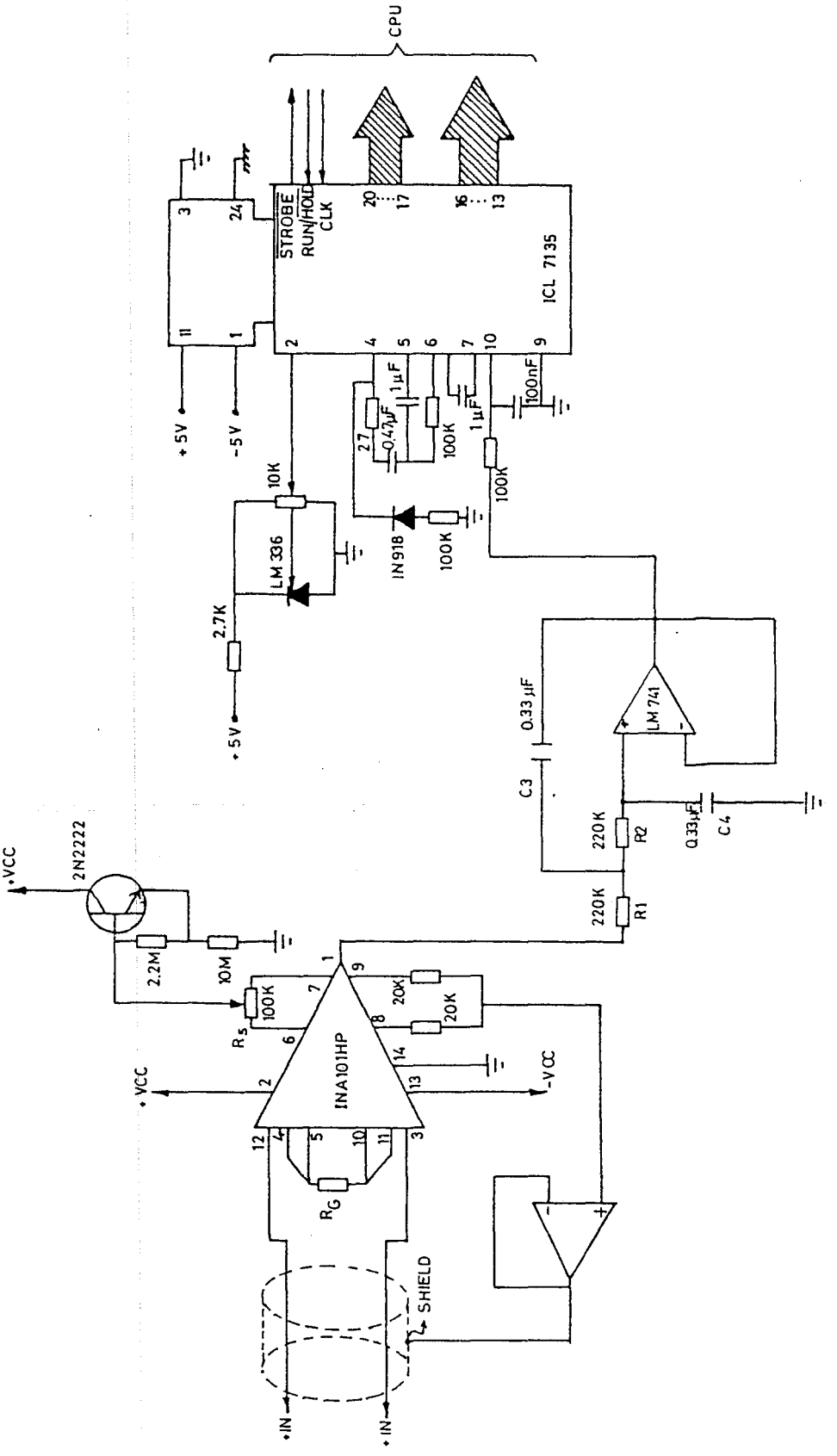
Bu saat işareti PIO-2'nin TIMER OUT'undan alınmıştır. Bilindiği gibi 8155'in programlanabilir bir sayıcı/zamanlayıcı'sı vardır. 8155 aşağıdaki şekilde programlanarak istenilen 125KHz elde edilmiştir.

```
MVI A,18H
OUT 54H
MVI A,40H
OUT 55H
MVI A,0F4H
OUT 50H
```

7135'in çıkıiı BCD formdadır. STROBE çıkışının her alçak seviyeye düşüşünde bir dijit için gerekli BCD veri, çıkışına yansımaktadır. 4½ dijitlik olmasından dolayı 5 dijit için BCD çıkış vermektedir. Yani 5 kez arka arkaya STROBE çıkışı gelmektedir. Bu çıkışlar yazılımla kontrol edilerek bir ölçüm için gerekli olan 5 adet BCD veri bellekte 5 byte'lık bir bölgeye alınmaktadır.

4.2 DVM ile Sistem Kalibrasyonu

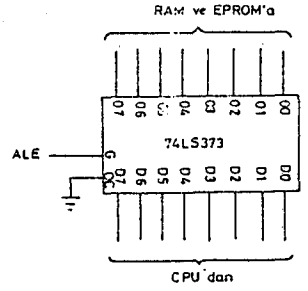
Şekil 4-2'de DVM ve yükselteç devresinin açık şeması verilmiştir. Kuvvetlendiricinin Rg kazanç direnci ile istenilen maksimum ağırlık kalibrasyonu yapılır. Yani 60t maksimum ağırlık ise Rg direnci göstergede 60.00 gözleninceye kadar ayarlanır. Bu şekilde A/D'nin üst kalıbrasyonu yapılmış olur. Kantar üzerinde hiç bir ağırlık yokken de göstergede 00.00 gözleninceye kadar Rs direnci ile ayar yapılır. Böylece alt kalibrasyon da yapılmış olur. Bu işlemlerden sonra kantar ölçüm yapmak için hazır duruma getirilmiş demektir.



Sekil 4.2 DVM ve Instrumantasyon Yükseltecin Baglantısı

5. DONANIM

Bu tez çalışmasında tasarlanan devrenin kontrolu 8085 mikroişlemcisi ile yapılmaktadır. Bu işlemci tek başına bir CPU'dur.Çünkü tek bir entegre içerisinde kendisi için gerekli clock ve kontrol devrelerini içermektedir. 16-bit'lik adres hattının Low Byte'nı (ilk 8 bitini) ALE sinyalinin durumuna göre hem data hattı hem de adres hattı olarak kullanmaktadır. Devrede adres data Latch olarak 74LS373 entegresi kullanılmıştır. Enable bacağına bağlanan ALE sinyalinin durumuna göre sürekli çıkış vermektedir. ALE sinyali Low ise AD0-AD7 hatlarından gelen bilgi tutulur. Bu bilgi data olarak görülür. ALE sinyali High ise AD0-AD7 hattından gelen bilgiye yol verir. EPROM ve RAM bu bilgiyi adres olarak görür. Bu şekilde ayrılan adres ve data sadece EPROM ve RAM'e gider.Diğer entegreler (8155 , 8279) ayırma işlemini kendi içinde yaparlar. Bu entegrelere sadece ALE sinyalini girmek yeterlidir. Şekil 5.1'de bu ayırma işlemi gösterilmiştir.



Şekil 5.1 Adres Veri Tutucu

8085'in RD çıkış bacağı aküMülatöre bilgi girişi olduğunu, WR çıkış bacağı ise aküMülatörden bilgi çıkışı olduğunu gösterir. Bu bilgi giriş ve çıkışının nereden ve nereye yapılacağı ise IO/M çıkış bacağının durumuna bağlıdır. Bu bacak High ise I/O portu ile, Low ise bellek ile bilgi alışverişi yapılacağı anlaşılır.

Ayrıca 8085'in 8 tane Software Interrupt'ı ve 4 tane de Hardware Interrupt'ı vardır. Sistem Hardware Interrupt bacaklarına gelen uygun sinyaller doğrultusunda her bir in-

terrupt için belirlenen adres bölgelerine dallanır.

Tasarlanan devrede 3MHz'lik clock sinyali kullanılmıştır. Sistem dışardan bağlanan 6MHz'lik bir kristal sayesinde bu clock sinyalini kendisi elde etmektedir. CPU kartının dış dünya ile alışverişini sağlamak için 2 tane 8155 PIO kullanılmıştır. Kartta hafıza birimi olarakta 8K'lık 2764 EPROM ve 8K'lık 6264 RAM vardır.

5.1 Mikroişlemci Devresi

Mikroişlemci devresi adres çözücü, bellek birimleri, giriş-çıkış birimleri ve tuş-gösterge birimlerinden oluşmaktadır. Devrenin açık şeması şekil 5.2'de gösterilmiştir.

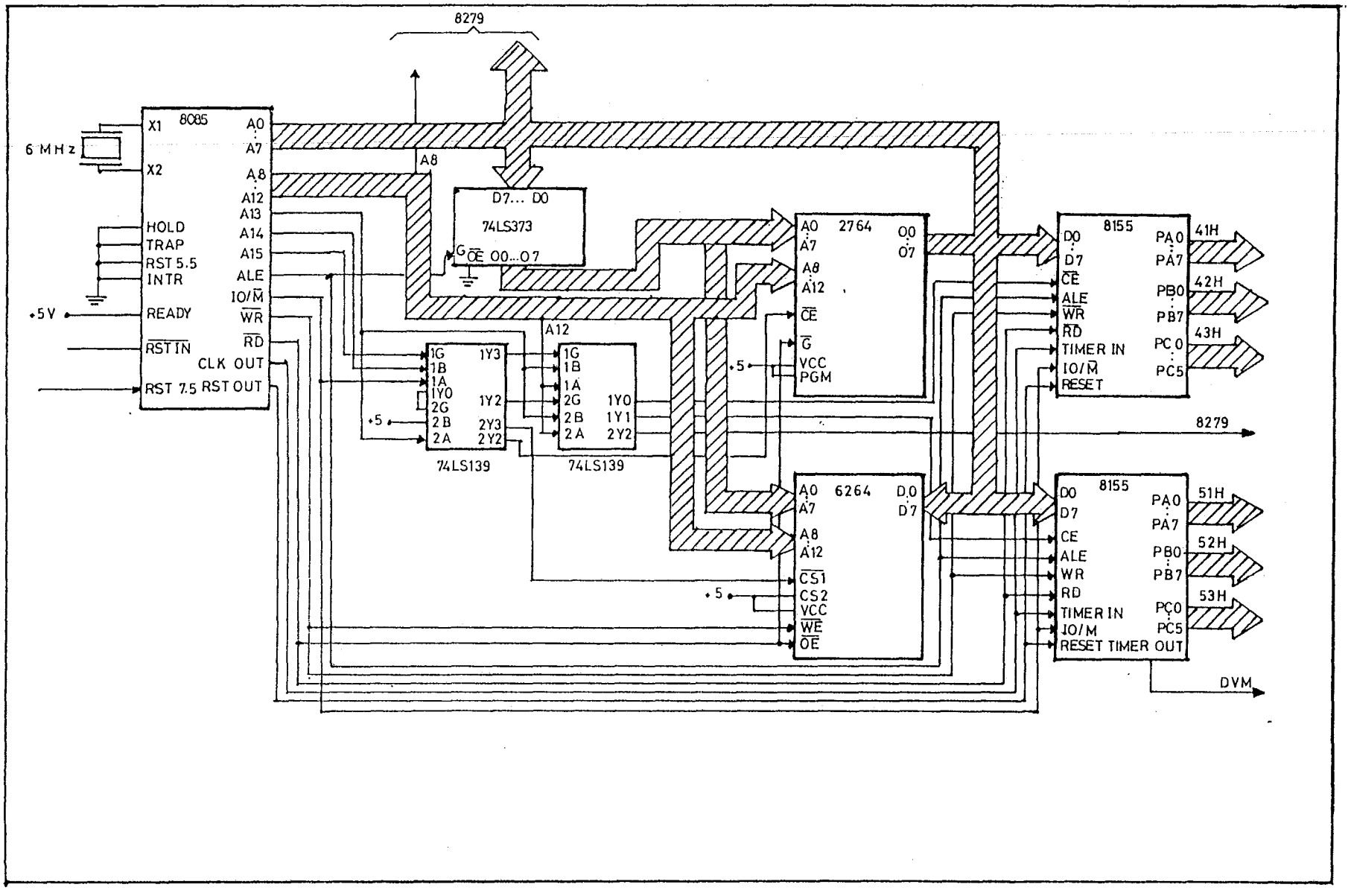
5.1.1 Bellek Haritası ve Adres Çözücü

Mikroişlemcinin aradığını yerinde bulabilmesi için 64K'lık maksimum kapasitesi belirli bölgelere ayrılmıştır.Bu şekilde mikroişlemci istediği zaman hafıza birimlerine ve çevre elemanlarına bir karışıklığa neden olmadan ulaşacaktır.

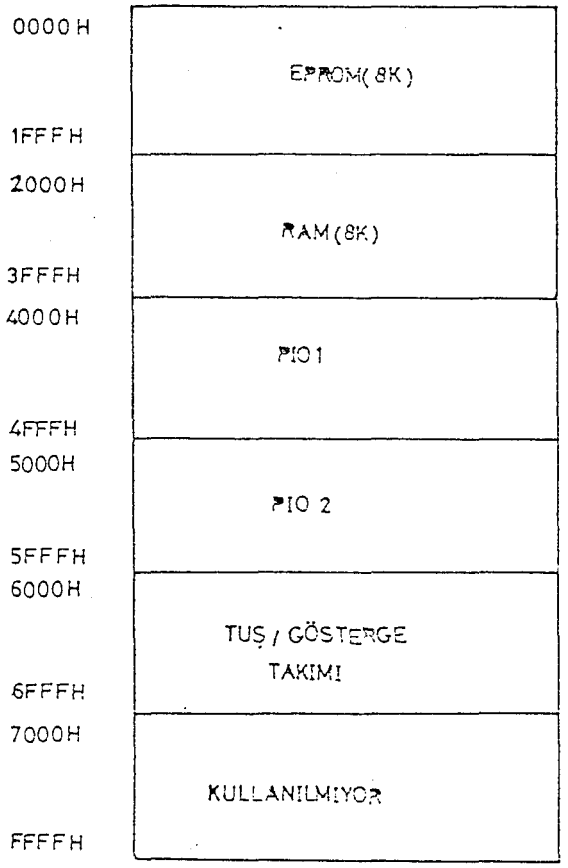
Tez çalışmasında bu durumu sağlayabilmek için önce bir bellek haritası çıkarılmıştır. Sonra bellek haritasına uygun bir adres çözücü devresi yapılmıştır. Şekil 5.3'de kullanılan bellek haritası gösterilmektedir.

Adres çözücü devresi iki tane 74LS139 2'den 4'e kod çözücü entegresi kullanılarak yapılmıştır. Girişlerine A15, A14, A13 ve A12 adres hatları uygun şekilde bağlanarak belek iki tane 8K'lık, üç tane 2K'lık bloklara bölünmüştür. Şekil 5.4'de bu işlemi yapan adres çözücü'nün şeması verilmiştir.

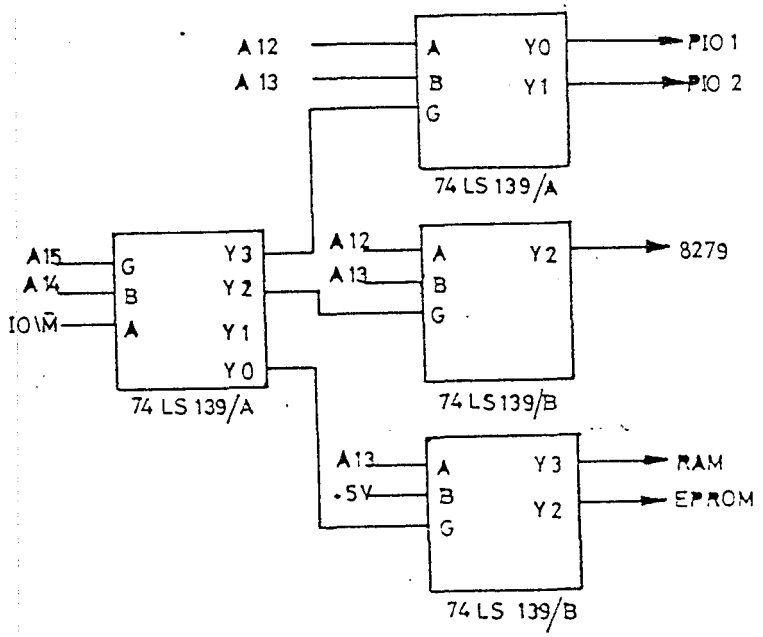
Eprom'da sistem programları ve sabit değerler saklanmıştır. RAM'de ise program akışı içerisinde gerekli ara değerler ile sabit olmayan değişkenler saklanmıştır. Ayrıca RAM yığıltıyı (stack) da gerçekleştirmiştir. Tasarlanan Elektronik Kantarda 100 araca kadar tarih, plaka ve ağırlık bilgileri RAM'de muhafaza edilebilmektedir.



Şekil 5.2 Mikroişlemci Devresi



Şekil 5.3 Bellek Haritası



Şekil 5.4 Adres Çözücü

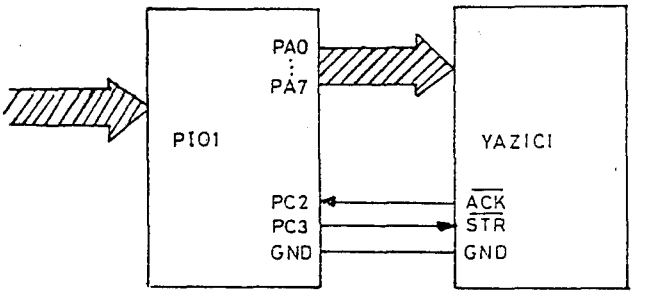
5.1.2 Giriş-Çıkış Birimleri

Yapılan devrede iki adet 8155 PIO'su kullanılmıştır. 8155'in iki tane 8'er bit programlanabilir Giriş/Çıkış portu, 1 tane 6 bit programlanabilir Giriş/Çıkış portu ve yine programlanabilir 14-bit'lik sayıcı/zamanlayıcısı vardır. Tasarlanan devrede 44-bit'lik Giriş/Çıkış portu mevcuttur. Bu portların kontrolu komut kütüğüne yazılan belirli kontrol kelimeleri ile sağlanır.

Sistemdeki PIO-1 yazıcı ile bağlantı sağlamak,PIO-2 ise ADC katından gelen ağırlık bilgisini okumak için kullanılmıştır.

5.1.3 Yazıcı ile bağlantı

Bir takım istatistiklerin tutulması için tartım sonuçlarının bir kağıda aktarılması gerekmektedir. Bu nedenle sistemin PIO-1'i yazıcı ile alış veriş yapmak için kullanılmıştır. Mikroişlemciden bilgiler yazıcıya paralel olarak gönderilmektedir. Yazıcı ile yapılan bağlantı Şekil 5-5'de gösterilmiştir.

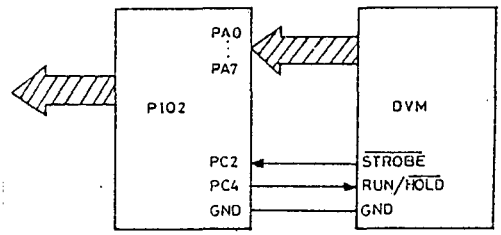


Şekil 5.5 Yazıcı İle Bağlantı

PIO-1'in A portu çıkışa C portu ise Alt-3'e programlanmıştır. PIO-1'in port numarası 40H'dir. Buna göre port-A 41H ve port-C 43H adresi ile seçilmektedir. Bu durumda 8-bit'lik C portunun PC0,PC1,PC2 bitleri protokol için PC3, PC4, PC5 bitleri ise çıkış olarak kullanılmaktadır. Protokol işleminin nasıl yapıldığı yazılım bölümünde detaylı olarak anlatılacaktır.

5.1.4 ADC ile baglantı

Load Cell'den gelen ağırlık bilgisi uygulanan kuvvetle orantılı olarak değişen ve milivoltlar seviyesinde olan bir doğru gerilimdir. Bu gerilimin mikroişlemciye alınıp işlenebilmesi için öncelikle sayısal hale getirilmesi gerekmektedir. Bu da 4½ digitlik 7135 DVM (Digital Voltmetre) entegresi kullanılarak gerçekleştirilmiştir. DVM'in çıkışları PIO-2'nin A portu üzerinden mikroişlemciye alınmaktadır. DVM ile yapılan bağlantı Şekil 5.6'da gösterilmiştir.



Şekil 5.6 DVM ile Baglantı

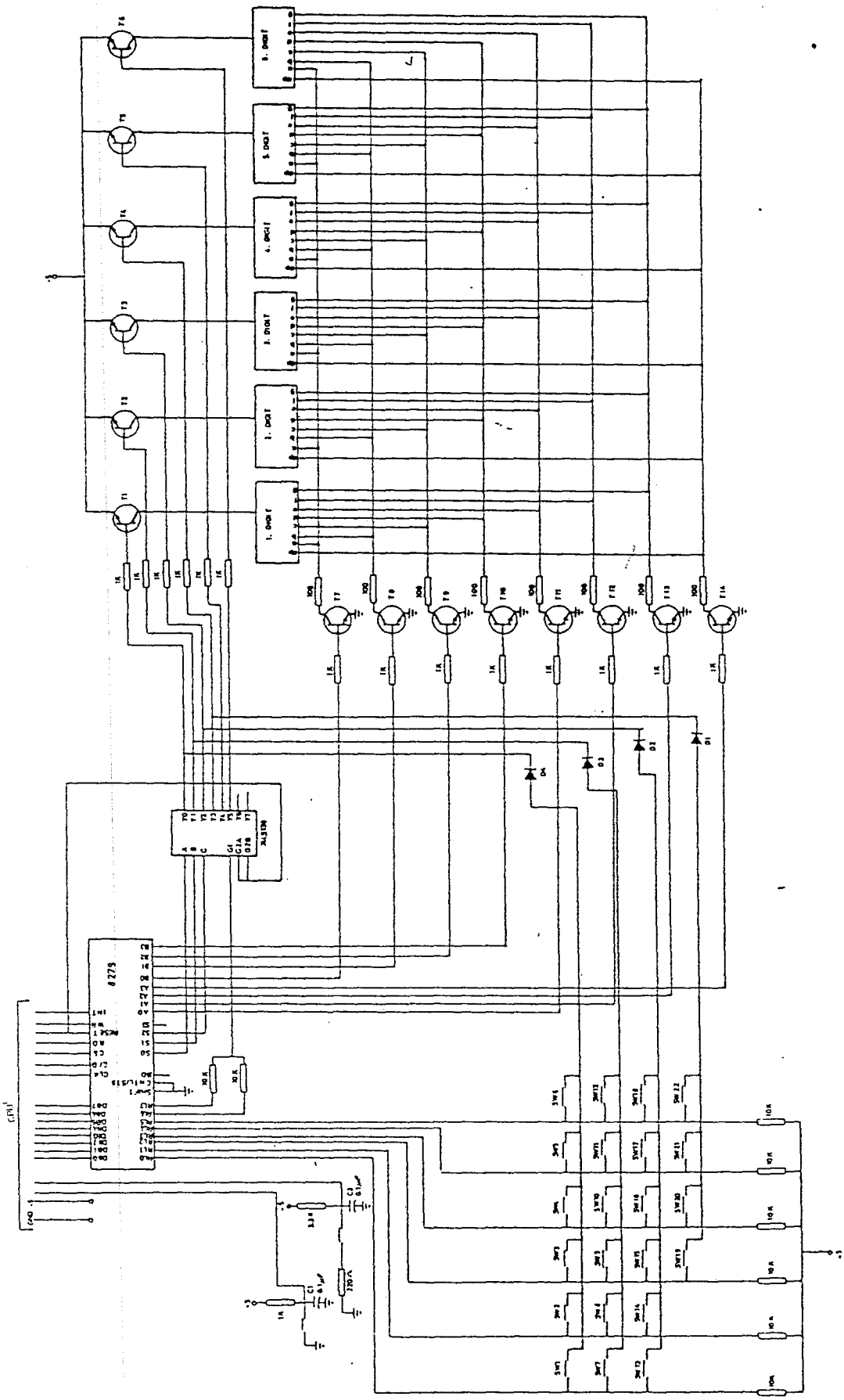
PIO-2'nin A portu girişe C portu'da Alt-3'e programlanarak DVM'den data kolayca okunmuştur. Yine burada da DVM ile yapılan protokol işlemi Yazılım konusunda anlatılacaktır.

5.2 Tuş ve Gösterge Devresi

Tuş ve Gösrerge takımına ait devrenin akış şeması şekil 5.7'de gösterilmektedir. Mikroişlemci için tuşlar bir giriş ünitesi göstergeler ise bir çıkış ünitesidir.

Yapılan elktronık kantar devresinin Tuş/Gösterge kartında programlanabilir Tuş/Gösterge ara birimi olarak bilinen 8279 entegresi kullanılmıştır. Bu entegre 8 adet 7-parçalı gösterge ve 64 ile 128'e kadar olan tus takımını kontrol edebilmektedir. Bu tezde sadece 6 adet 7-parçalı gösterge ve 24 adet tuş kullanılmıştır.

8279'un C/D bacağına A8 adres biti bağlanmıştır. 8279 A8 bitinin değişimine göre bus'taki bilgiyi ya veri ya da

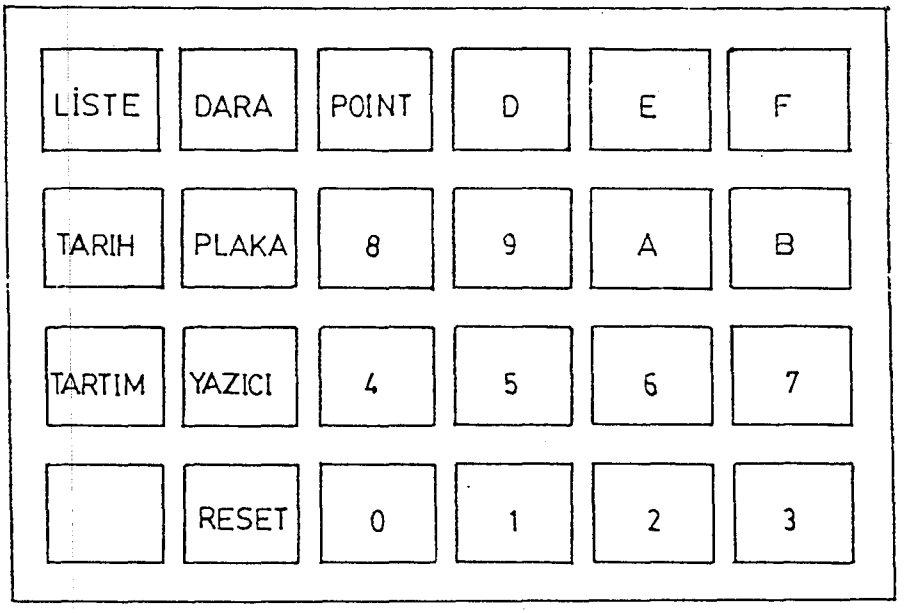


Şekil 5.7 Tuş ve Gösterge Devresi

komut olarak kabul etmektedir. A8 lojik 1 seviyesinde ise data bus'taki bilgi komut, lojik 0 seviyesinde ise data olarak algılanmaktadır.

5.3.1 Tuş Takımı

Devrede kullanılan 24 tuşun yerleşim planı Sekil 5.8'de gösterilmiştir. 8279 bir 8x8 FIFO/SENSOR RAM'ine sahiptir. 8279'un herhangi bir tuşuna basıldığında o tuşa ait olan kod FIFO/SENSOR RAM'e yazılır. Tuşa basıldıgı anda 8279'un INT kısa bir süre için lojik 1 seviyesine çıkar. Yapılan devrede bu INT bacağı 8085'in RST 7.5 bacağına bağlanmıştır. Böylece bir tuşa basıldığı zaman mikrıişlemci 003CH adresine dallanır. Orada yazılmış olan bir program aracılığıyla 8279'dan tuşun kodu mikroişlemci içine okunarak sistem RAM'inde KEY ile temsil edilen 2000H adresine yazılır.



Şekil 5.8 Tuşların yerleşimi

5.3.2 Gösterge Takımı

Devrede 6 adet 7-parçalı gösterge kullanılarak bir gösterge yapılmıştır. 8279 bir 16x8 Gösterge RAM'ine sahiptir. Bu RAM'e Şekil 5.9'daki formda yazılan bilgiler ilgili komut kullanılarak doğrudan göstergede görülür.

D7	D6	D5	D4	D3	D2	D1	D0
dp	g	f	e	d	c	b	a

Şekil 5.9 8279 için 7-parça formatı

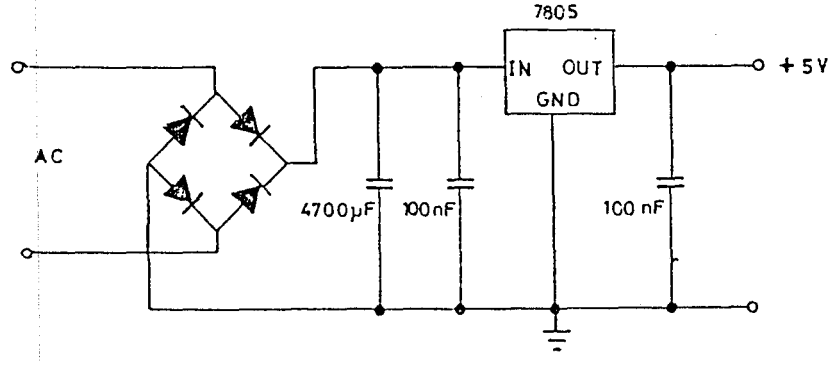
Bu RAM'e hem sağdan hemde soldan bilgi yazılabilir. Aşagıdaki program örneğinde 8279'un nasıl programlandığı ve göstergeye datanın nasıl gönderildiği açıklanmıştır. Adres çözücü tasarlanırken 8279'un komut adresi 6100H, veri adresi de 6000H olarak tayin edilmişti.

```
LXI H,6100H
MVI M,02H
MVI M,90H
DCX H
MVI M, 0F6H
MVI M, 78H
MVI M, 5CH
MVI M, 50H
MVI M, 0DCH
MVI M, 76H
```

Programda; komut olarak 02H gönderildiğinde gösterge soldan girişe, tuşlarda Encoded Scan Keyboard-N Key Roll-over'a kurulmuş olmaktadır. 90H komutu ise veri olarak gelecek olan ilk bilgiyi Display RAM'e soldan ilk dijite yaz. ondan sonra gelecek olan bilgiyi soldan ikinci dijite yaz anlamına gelmektedir. Bu işlem tüm dijitler soldan itibaren doluncaya kadar devam eder.

5.4 Güç Kaynagı

Mikroişlemci ve Tuş/Gösterge devreleri +5V'luk bir dc kaynak ile beslenmektedir. Bu kaynak 7805 regüle entegresi kullanılarak yapılmıştır.Şekil 5.10'da güç kaynagı devresi gösterilmiştir.



Şekil 5.10 Güç Kaynagı

6.YAZILIM

Sistem programları 8085 mikroişlemci komutları ile gerçekleştirilmiştir. Programlar tarih ve plaka bilgilerinin tuşlar aracılığıyla girilmesi, ağırlık bilgisinin ADC'den okunması, istenilen bilgilerin yazıcıya aktarılması gibi imkanları sağlayan alt programlar şeklinde yazılmıştır.

6.1 Ana Program (Tuş Tanıma)

Bu programın akış diyagramı Şekil 6-1'de gösterilmiştir. Sisteme güç verildiği andan itibaren bu program aracılığıyla gösterge test edilir. Test işlemi göstergedeki tüm dijitlerde 9'dan 1'e doğru sayma yaptırarak sağlanmıştır. Sayım işleminden sonra göstergede "ready" mesajı gösterilmektedir. Bu mesajdan sonra sistem bir tuşa basılıncaya kadar beklemektedir. Herhangi bir tuşa basıldığı anda program RST 7.5 interrupt'ına ait olan 003CH adresine giderek o tuşa ait olan kodu 8279'un FIFO/SENSOR RAM'inden okuyarak 2000H adresine atar. Sonra o basılan tuşun ilgili olduğu alt programı yürütür.

6.2 Tarih Programı

Yapılan tartım sonuçlarının günlük sıraya konulabilmesi için tarih bilgisinin de girilmesi gerekmektedir. Şekil 6-2 de tarih alt programının akış diyagramı verilmiştir. Bu program tarih tuşuna basıldığı andan itibaren çalıştırılır. İlk olarak göstergede "date" mesajı gösterilir. Daha sonra 6 dijitlik tarih tuşlar kullanılarak girilir. Ancak yılın sadece son iki rakamı girilebilmektedir. Örneğin 2. ayın 4'ünde bir tartım yapılmış olsun. Bu bilgi göstergede ve yazıcıda şu şekilde gözlenecektir:

040290

6.3 Plaka Programı

Hangi aracın tartıldığı plakasına bakılarak ayırt edilebilmektedir. Şekil 6-3'de plaka alt programının akış diyagramı

verilmiştir. Plaka tuşuna basıldığında bu alt program yürütülür. İlk olarak göstergede "Plaka" mesajı gösterilir. Daha sonra program plakanın girilmesini bekler. Plaka bilgisi önce il kodu sonra da seri numarası şeklinde girilir. Harflerin girilmesine gerek duyulmamıştır. Örneğin 26AD525 plakalı araç tartılmış olsun. Bu bilgi gösterge ve yazıcıda şu şekilde gözlenecektir:

260525

6.4 Yazıcı Programı

Cihaz bir yazıcı ile birlikte çalışmaktadır. Yazıcıya ihtiyaç duyulmasının sebebi sonuçların yazılı olarak alınmak istenmesidir. Şekil 6-4'de yazıcı alt programının akış şeması verilmiştir.

Yazıcıya yazılacak olan veriler öncelikle bellekte bir bölgeye alınır. Yazıcı hazır olduğu sürece bellekten yazıcıya bilgi PIO yardımıyla aktarılır. PIO'dan yazıcıya "bilgiyi gönderdim" sinyali yollanır. Yazıcı da bilgiyi aldığı zaman PIO'ya "bilgiyi aldım" sinyali yollar. Bu sinyal PIO'dan geçerek mikroişlemciye ulaşır. Bunun üzerine mikroişlemci de yeni bir bilgi yollar. Bu işlem bellekte yazılacak karakterler bitinceye kadar devam eder. Yapılan bir tartım sonucunda kağıda yazdırılacak olan bilgi şu şekilde olacaktır:

030290 260676 043.050 t

6.5 Başlık Programı

Yazıcıya yazdırılan bilgilerin neyi temsil ettiğini belirtmek için her bilgiye ait birer etiket vermek ihtiyacı duyulmuştur. Şekil 6-5'te başlık alt programına ait akış şeması gösterilmektedir.

Bu alt program yürütüldüğünde yazıcıdan;

TARİH PLAKA TARTIM

formunda bir çıktı alınır. Başlık verileri EPROM'da 07A0H adresinden itibaren ASCII kodları şeklinde saklanmıştır.

6.6 Liste Programı

Bu program yapılan tüm tartım sonuçlarının tarih ve plaka bilgileri ile birlikte yazıcıdan alınması imkanını verir. Şekil 6-6'da liste alt programının akış şeması verilmiştir. Tartım programı toplam 100 aracın tartımını yapacak şekildde hazırlanmıştır. O halde 100 aracın tartım sonuçları bu alt program yardımıyla elde edilebilmektedir.

6.7 Tartım Programı

Bu alt programın akış şeması Şekil 6-7'de verilmiştir. Tartım tuşuna basılarak program yürütülür. İlk önce göstergede "tart" mesajı gösterilir. Sonra da tartma işlemi yaptırılır. Her ağırlık bilgisi belleğin 2406H adresinen başlamak üzere 5 byte'lık bölgede depo edilir. Daha sonra bu bilgi binary'e çevrilerek 240EH ve 240FH adreslerine saklanır. Bu ölçülen ağırlık daradan çıkartılarak net ağırlık 2410H ve 2411H adreslerine alınır. Daha sonra net ağırlık BCD'ye çevrilerek göstergede ton olarak göstertilir. Ölçülmüş olan bir aracın ağırlığı göstergede şu şekilde gözlenir:

01.78t

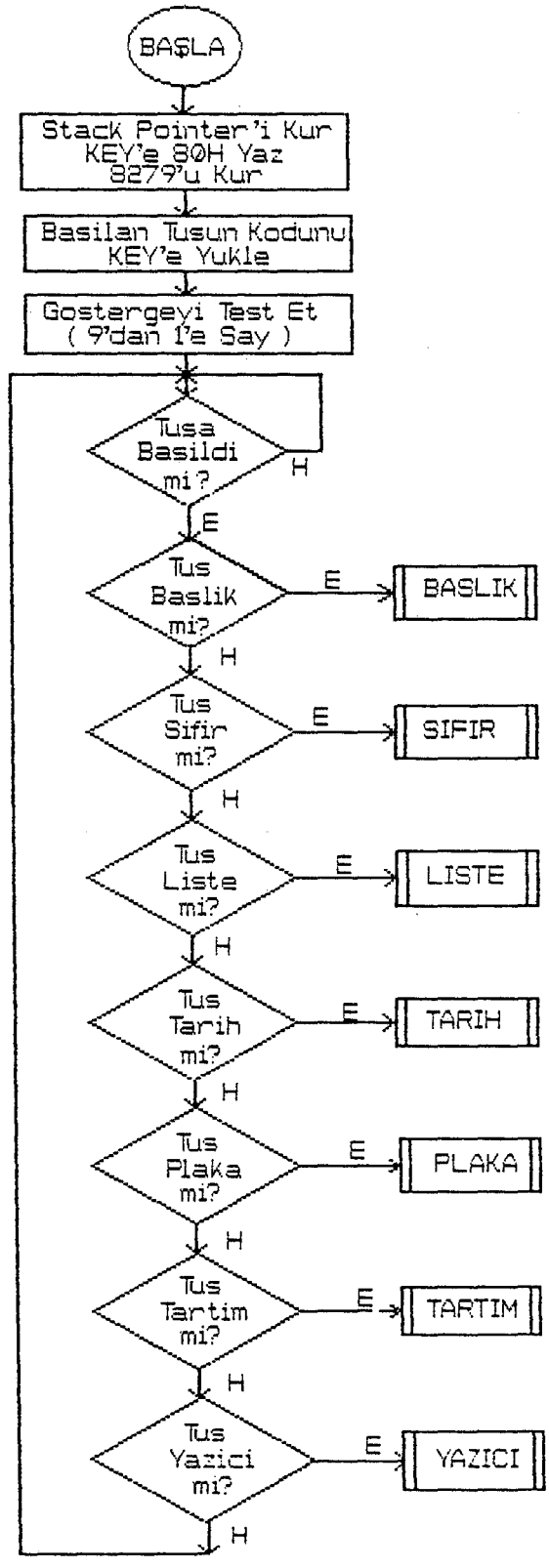
Ölçme işleminde mikroişlemciden DVM'e "Ağırlığı ölç" sinyali gönderilir. DVM de ölçme işlemi bitince mikroişlemciye "ölçtüm ve yeni bir ağırlık işlemine hazırım" şeklinde bir sinyal gönderir. Bu karşılıklı haberleşme her tartımda yapılır.

6.8 Dara Programı

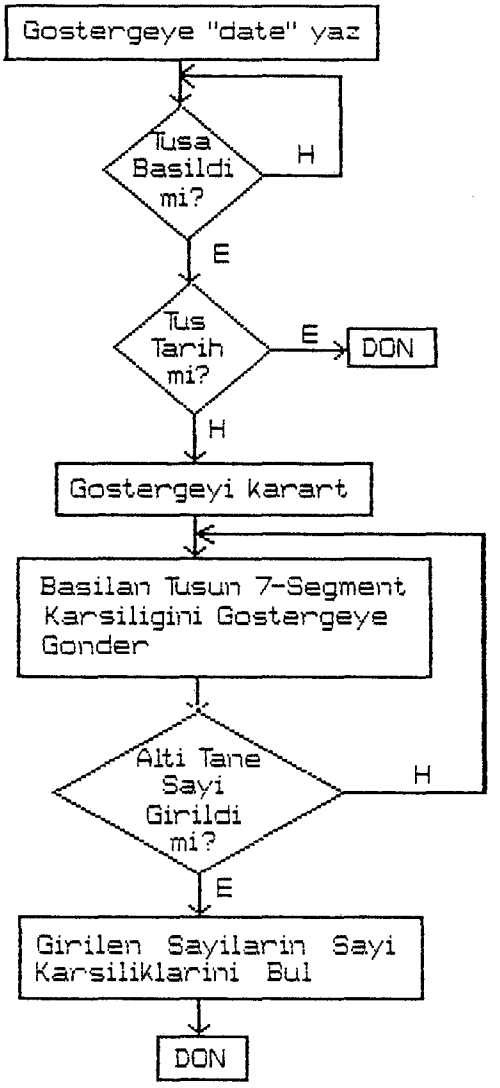
Bir aracın net ağırlığının ölçülebilmesi için ilk olarak kantarın platform ve üzerinde bulunan artık maddelerin ağırlığının okunması gerekmektedir. Yani dara ölçülme ve bellekte bir bölgede saklanmalıdır. Böylece her yeni bir tartımda dara bilgisi alınarak aracın net ağırlığı hesaplanabilir. Dara alt programına ait akış diyagramı şekil 6-8'de gösterilmiştir.

Ağırlık bilgisi PIO-2'nin A portu üzerinden mikroişlem-

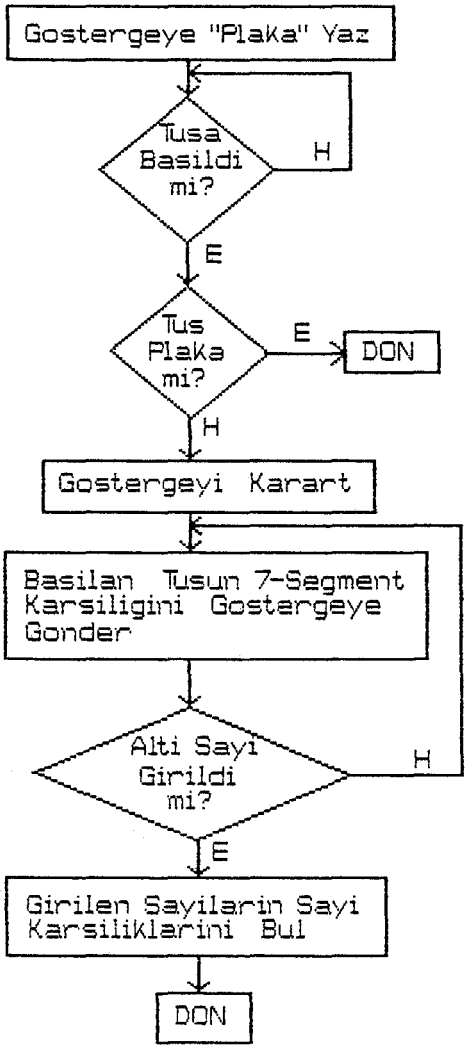
ciye alınır. DVM çıkışı BCD formda olduğu için bir ağırlık bilgisi bellekte 5 byte'lık bir bölgeyi işgal etmektedir. Bu bölge 2400H adresinden itibaren başlamaktadır. Daha sonra bu BCD binary'e çevrilerek 240CH ve 240DH adreslerine yerleştirilmiştir. Program bu işlemleri yaptıktan sonra göstergedeki tüm dijitleri sıfırlayarak tartıma hazır olduğunu bildirir.



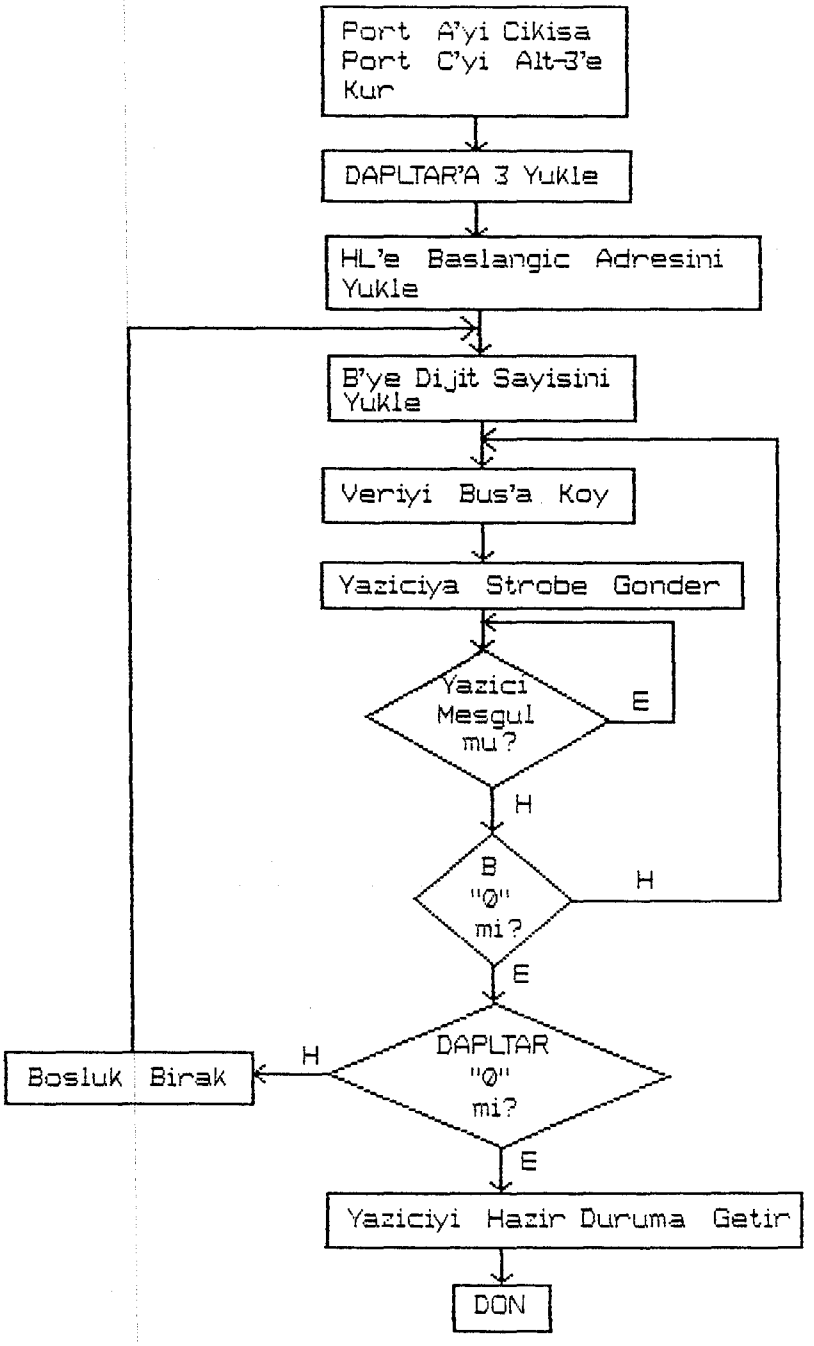
Sekil 6.1 Ana Program Akis Diyagrami



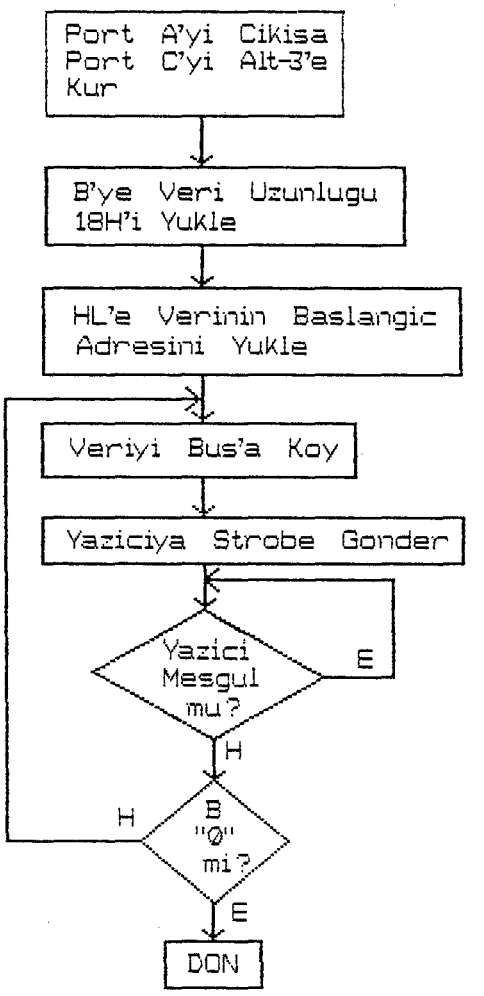
Sekil 6.2 Tarih Programi Akis Diyagrami



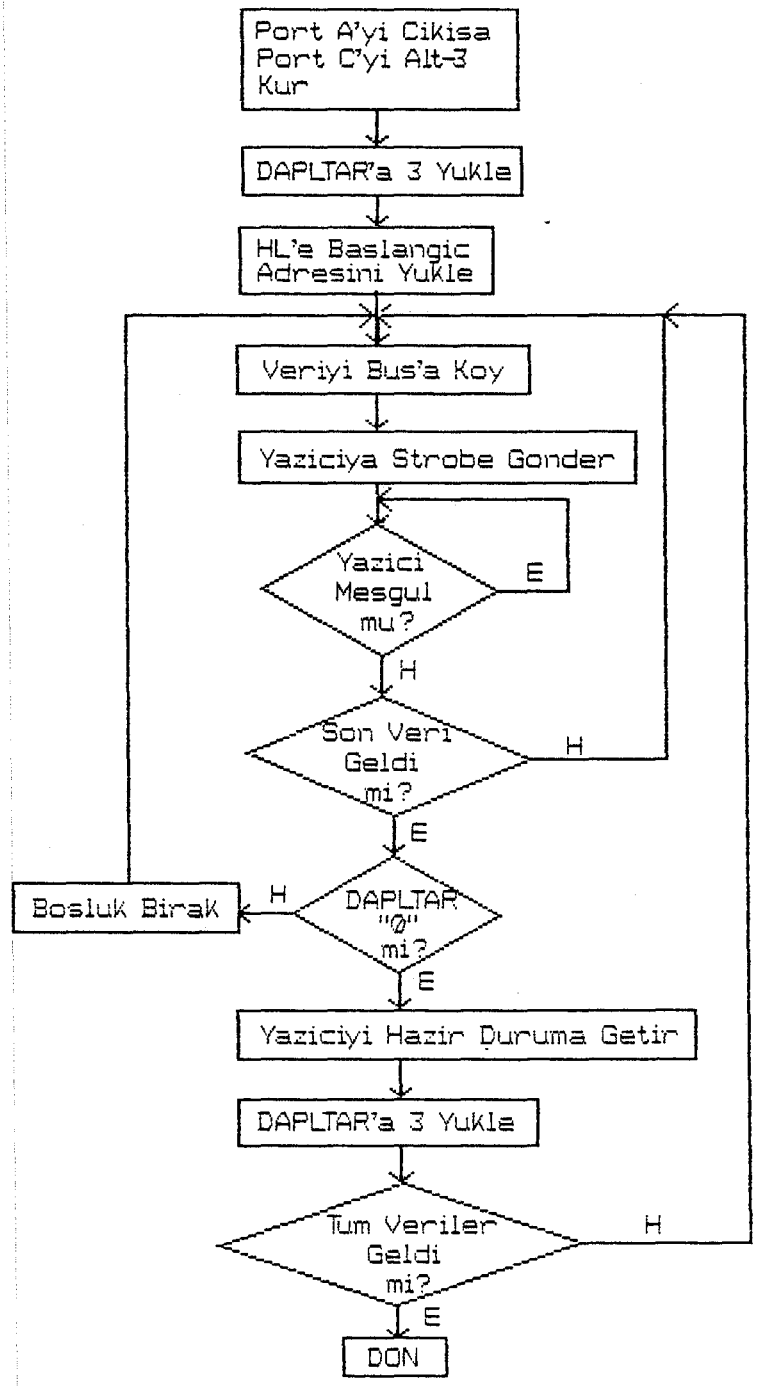
Sekil 6.3 Plaka Programi Akis Diyagrami



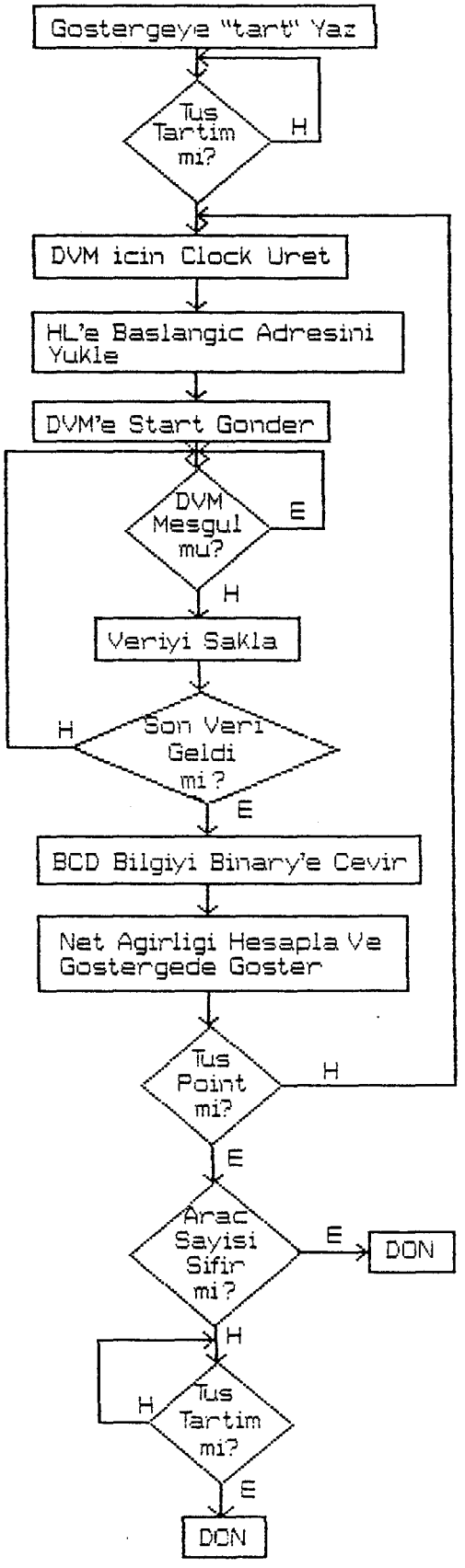
Sekil 6.4 Yazici Programi Akis Diyagrami



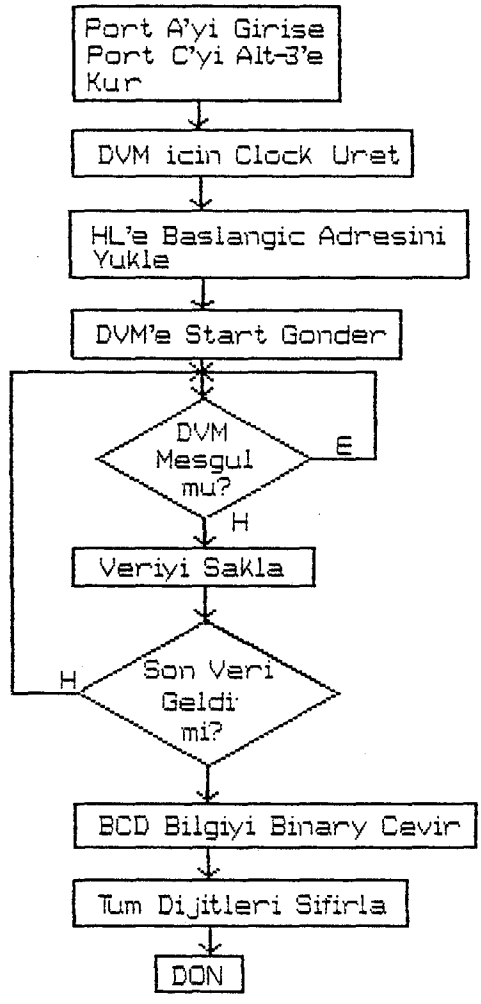
Sekil 6.5 Baslik Programi Akis Diyagrami



Sekil 6.6 Liste Programi Akis Diyagrami



Şekil 6.7 Tartim Programi Akis Diyagrami



Sekil 6.8 Dara Programi Akis Diyagrami

7. SONUÇ ve ÖNERİLER

Ülkemizde günümüze kadar analog tipte kantarlar yapılmakta ve kullanılmaktaydı. Son üç dört yıl içerisinde elektronik kantar kullanımı ve isteği artmıştır. Ancak bu kantarların devreleri yabancı ülkelerden ithal edilip sadece montajı ülkemizde yapılmaktadır. Bu çalışmada tonaj mertebesinde ağırlık ölçen mikroişlemci kontrollu elektronik kantar devresi tasarlanmıştır. Ağırlık artış aralığı 10 Kg olarak ayarlanmıştır. Bu aralık bütün ölçümlerde sabit kalmaktadır. Yapılan devre Eskişehir'de TÜLOMSAŞ fabrikasındaki 60t'luk bir kantarda denenerek hatasız ağırlık ölçümleri alınmıştır.

Sistem program esnekliğine sahiptir. EPROM'daki boş yerler ve tuş takımındaki tuşlar kullanılarak değişik fonksiyon işlemleri yaptırılabilir. Gösterge olarak LCD display kullanılabilir. Alfa nümerik bir sistem haline getirilebilir. Ayrıca bir bilgisayara bağlantı yapılabilir. Diğer taraftan 5½ dijitlik DVM'ler veya yüksek hassasiyetli (yüksek resolution) ADC'ler kullanılarak daha hassas ölçümler yapılabilir.

KAYNAKLAR

1. Malvino, Albert Paul,"Digital Computer Electronics", McGraw-Hill Book Co.,1983,Sayfa:195-280.
2. Hall, Dougles V., "Microprocessors and Digital Systems", McGraw-Hill Book Co.,1983,Sayfa:312-319
3. 8085 Microcomputer Systems User's Manual INTEL
4. Coughlin, Robert F. ve Driscoll, Frederick F., "Operational Amplifiers and Linear Integrated Circuits" Prentice-Hall,Inc.,1987,Sayfa:190-198,209-212,215-219.
5. Allocca, John A. ve Stuart, Allen,"Transducers Theory and Applications", Reston Publishing Company, Inc.,1984, Sayfa:29-67.

MİKROİŞLEMCİ KONTROLLU AĞIRLIK ÖLÇME SİSTEMİ

EKLER

EK-1..PROGRAMLAR

EK-2..KULLANILAN ENTEGRE DEVRELER

EK-3..BASKILI DEVRE ŞEMALARI

ŞUBAT-1990

EK-1

```
KEY       EQU 2000H
TARIH     EQU 2002H
PLAKA     EQU 2008H
AGRO      EQU 200EH
OFFST1    EQU 2400H
WGT1      EQU 2406H
DEPO1     EQU 240CH
DDEP01    EQU 240EH
NET1      EQU 2410H
NET2      EQU 2411H
PTARIH    EQU 2412H
PPLAKA    EQU 2414H
PAGIR     EQU 2416H
DAPLTAR   EQU 2418H
ARAC      EQU 2419H
INCR      EQU 0700H
DATA      EQU 07A0H
          LXI SP,3FFFH
          MVI A,0BH
          DB 30H
          EI
          LXI H,KEY
          MVI M,80H
          LXI H,8100H
          MVI M,12H
          MVI M,96H
          DCR H
          MVI M,0F6H
          MVI M,78H
          MVI M,5CH
          MVI M,50H
          MVI M,0DCH
          MVI M,7EH
          CALL TIMING
          JMP YASAK
          ORG 003CH
          PUSH H
          PUSH PSW
          LXI H,8100H
          MVI M,40H
          DCR H
          MOV A,M
          STA KEY
          POP PSW
          POP H
          RET
YASAK:    LXI H,ARAC
          MVI M,64H
          LXI H,00H
```

```
          SHLD PTARIH
          SHLD PPLAKA
          SHLD PAGIR
L4AP:     MVI B,09H
L4AOP:    MVI C,06H
          EI
          MOV L,B
          MVI H,11H
TEST:     MOV A,M
          STA 6000H
          DCR C
          JNZ TEST
          CALL TIMING
          DCR B
          JNZ L4AOP
          LXI H,6000H
          MVI M,50H
          MVI M,79H
          MVI M,77H
          MVI M,3FH
          MVI M,6EH
          MVI M,00H
TUS:      LDA KEY
          CPI 00H
          CZ BASLIK
          CPI 01H
          CZ SIFIR
          CPI 03H
          CZ LISTE
          CPI 08H
          CZ L1
          CPI 09H
          CZ L2
          CPI 10H
          CZ L3
          CPI 11H
          CZ L4
          LXI H,KEY
          MVI M,00H
          EI
          LXI H,6000H
          MVI M,50H
          MVI M,79H
          MVI M,77H
          MVI M,3FH
          MVI M,6EH
          MVI M,00H
TUSSS:    LDA KEY
          CPI 00H
          JZ TUSSS
          JMP TUS
L1:       LXI H,8000H
          MVI M,00H
          MVI M,5EH
          MVI M,77H
```

```
        MVI M,79H
        MVI M,79H
        MVI M,00H
        LXI H,KEY
        MVI M,80H
        EI
SIL1:   MOV A,M
        CPI 80H
        JZ SIL1
        CPI 08H
        JZ DONEMI
        MVI A,00H
        MVI B,06H
SIL2:   STA 6000H
        DCR B
        JNZ SIL2
        MVI B,06H
        LXI D,TABIH
        PUSH H
        LHLD PTARIH
        DAD D
        XCHG
        POP H
L4AP1:  MOV A,M
        CPI 80H
        JZ L4AP1
        XCHG
        MOV M,A
        XCHG
        PUSH D
        MOV E,A
        MVI D,10H
        XCHG
        MOV A,M
        XCHG
        STA 6000H
        POP D
        INX D
        MVI M,80H
        EI
        DCR B
        JNZ L4AP1
        MVI B,08H
        LXI D,TABIH
        LHLD PTABIH
        DAD D
LOOP3:  MOV E,M
        MVI D,12H
        XCHG
        MOV A,M
        XCHG
        MOV M,A
        INX H
        DCR B
        JNZ LOOP3
```

```
          CALL TIMING
DONEMI:   MVI A,80H
          STA KEY
          EI
          RET
L2:       LXI H,6000H
          MVI M,73H
          MVI M,38H
          MVI M,77H
          MVI M,76H
          MVI M,77H
          MVI M,00H
          LXI H,KEY
          MVI M,80H
          EI
SIL3:     MOV A,M
          CPI 80H
          JZ SIL3
          CPI 09H
          JZ DONEM1
          MVI A,00H
          MVI B,06H
SIL4:     STA 6000H
          DCR B
          JNZ SIL4
          MVI B,06H
          LXI D,PLAKA
          PUSH H
          LHLD PPLAKA
          DAD D
          XCHG
          POP H
LOOP4:    MOV A,M
          CPI 80H
          JZ LOOP4
          XCHG
          MOV M,A
          XCHG
          PUSH D
          MOV E,A
          MVI D,10H
          XCHG
          MOV A,M
          XCHG
          STA 6000H
          POP D
          INX D
          MVI M,80H
          EI
          DCR B
          JNZ LOOP4
          MVI B,06H
          LXI D,PLAKA
          LHLD PPLAKA
          DAD D
```

```
LOOP5:  MOV E,M
        MVI D,12H
        XCHG
        MOV A,M
        XCHG
        MOV M,A
        INX H
        DCR B
        JNZ LOOP5
        CALL TIMING
DONEM1: MVI A,80H
        STA KEY
        EI
        RET
L3:     LXI H,6000H
        MVI M,00H
        MVI M,78H
        MVI M,5CH
        MVI M,50H
        MVI M,78H
        MVI M,00H
        LXI H,KEY
        MVI M,80H
        EI
HC0:    MOV A,M
        CPI 10H
        JNZ HC0
HC1:    EI
        MVI A,18H
        OUT 54H
        MVI A,40H
        OUT 55H
        MVI A,0F4H
        OUT 50H
        EI
        LXI H,WGT1
        MVI B,05H
        MVI A,10H
        OUT 53H
T0:     IN 50H
        ANI 02H
        JZ T0
        IN 51H
        ANI 0FH
        MOV M,A
        INX H
        DCR B
        JNZ T0
        MVI A,74H
        OUT 50H
        LXI H,WGT1
        INX H
        LXI D,DDEP01
        CALL CEVIR
        INX D
```

```
          INX H
          CALL CEVIR
          LXI H,DEPO1
          INX H
          LXI D,DDEPO1
          INX D
          LDAX D
          CMP M
          JC ILAVE
          SUB M
          STA NET1
          DCX H
          DCX D
          LDAX D
          SUB M
          STA NET2
          JMP BCD
ILAVE:    SUB M
          ADI 64H
          STA NET1
          DCX H
          DCX D
          LDAX D
          SUB M
          DCR A
          STA NET2
BCD:      LXI H,NET1
          INX H
          LXI D,AGRO
          PUSH H
          LHLD PAGIR
          DAD D
          XCHG
          POP H
          MVI A,00H
          STAX D
          INX D
          CALL CCEVIR
          DCX H
          INX D
          CALL CCEVIR
          CALL DISPL
          LXI D,AGRO
          LHLD PAGIR
          DAD D
          MVI D,00H
          MVI E,05H
          DAD D
          MVI M,00H
          LDA KEY
          CPI 02H
          JNZ HC1
          LDA ARAC
          DCR A
          STA ARAC
```

```
          JZ RESET
          LHLD PTARIH
          CALL ARTIR
          SHLD PTARIH
          LHLD PPLAKA
          CALL ARTIR
          SHLD PPLAKA
          LHLD PAGIR
          CALL ARTIR
          SHLD PAGIR
          JMP HAMSI
RESET:    MVI A,84H
          STA ARAC
          LXI H,00H
          SHLD PTARIH
          SHLD PPLAKA
          SHLD PAGIR
HAMSI:    EI
WHAT:     LDA KEY
          CPI 10H
          JNZ WHAT
          LXI H,6100H
          MVI M,12H
          MVI M,96H
          MVI A,80H
          STA KEY
          EI
          RET
CCEVIR:   MVI B,0FFH
          MVI C,0AH
          MOV A,M
YO:       INR B
          SUB C
          JP YO
          ADI 0AH
          PUSH H
          MOV L,A
          MOV A,B
          STAX D
          INX D
          MOV A,L
          STAX D
          POP H
          RET
DISPL:    LXI H,8100H
          MVI M,02H
          MVI M,80H
          LXI D,AGRO
          LHLD PAGIR
          DAD D
          SUB A
          STA 8000H
          INX H
          CALL CONV
          INX H
```

```
          MOV A,M
          XCHG
          MVI H,11H
          MOV L,A
          MOV A,M
          ORI 80H
          STA 6000H
          XCHG
          INX H
          CALL CONV
          INX H
          CALL CONV
          LXI H,6100H
          MVI M,95H
          MVI A,78H
          STA 6000H
          RET
CONV:     MOV A,M
          XCHG
          MVI H,11H
          MOV L,A
          MOV A,M
          STA 6000H
          XCHG
          RET
ARTIR:    XCHG
          LHLD INCR
          DAD D
          RET
L4:       LXI H,KEY
          MVI M,80H
          EI
          MVI A,85H
          OUT 40H
          MVI A,03H
          STA DAPLTAR
          LXI D,TARIH
          LHLD PTARIH
          SUB A
          MVI C,12H
          SUB C
          MOV C,A
          MVI B,0FFH
          DAD B
          DAD D
TEKRAR:   MVI B,08H
PRT:      MOV A,M
          ADI 30H
          OUT 41H
          CALL 2F
          INX H
          DCR B
          JNZ PRT
          LDA DAPLTAR
          DCR A
```

```
          STA DAPLTAR
          JNZ BOSLUK
          MVI A,20H
          OUT 41H
          CALL BF
          MVI A,74H
          OUT 41H
          CALL BF
          MVI A,0BH
          OUT 41H
          CALL BF
          MVI A,80H
          STA KEY
          EI
          RET
BOSLUK:   MVI A,20H
          OUT 41H
          CALL BF
          MVI A,20H
          OUT 41H
          CALL BF
          JMP TEKRAR
BF:       SUB A
          OUT 43H
          MVI A,08H
          OUT 43H
C1:       IN 40H
          ANI 02H
          JNZ C1
          RET
BASLIK:   MVI A,35H
          OUT 40H
          MVI B,18H
          LXI H,DATA
DT:       MOV A,M
          OUT 41H
          CALL BF
          INX H
          DCR B
          JNZ DT
          MVI A,80H
          STA KEY
          EI
          RET
LISTE:    LXI H,KEY
          MVI M,80H
          EI
          MVI A,35H
          OUT 40H
          MVI A,03H
          STA DAPLTAR
          LXI H,TARIM
          MVI C,0A4
AGAIN:    MVI B,08H
PRNT:     MOV A,M
```

```
          ADI 30H
          OUT 41H
          CALL BF
          INX H
          DCR B
          JNZ PRNT
          LDA DAPLTAR
          DCR A
          STA DAPLTAR
          JNZ EMTY
          MVI A,20H
          OUT 41H
          CALL BF
          MVI A,74H
          OUT 41H
          CALL BF
          MVI A,0BH
          OUT 41H
          CALL BF
          MVI A,03H
          STA DAPLTAR
          DCR C
          JNZ AGAIN
          MVI A,80H
          STA KEY
          EI
          RET
EMTY:     MVI A,20H
          OUT 41H
          CALL BF
          MVI A,20H
          OUT 41H
          CALL BF
          JMP AGAIN
SIFIR:    LXI H,KEY
          MVI M,80H
          EI
          MVI A,18H
          OUT 54H
          MVI A,40H
          OUT 55H
          MVI A,0F4H
          OUT 50H
          LXI H,0FF0T1
          MVI B,05H
          MVI A,10H
          OUT 53H
SO:       IN 50H
          ANI 02H
          JZ SO
          IN 51H
          ANI 0FH
          MOV M,A
          INX H
          DCR B
```

```
          JNZ SO
          MVI A,74H
          OUT 50H
          LXI H,OFFST1
          INX H
          LXI D,DEPO1
          CALL CEVIR
          INX D
          INX H
          CALL CEVIR
          MVI C,06H
N1:       MVI A,3FH
          STA 6000H
          DCR C
          JNZ N1
          LDA KEY
          CPI 80H
          JZ N1
          MVI A,80H
          STA KEY
          EI
          RET
CEVIR:    ORA A
          MOV A,M
          RAL
          MOV C,A
          RAL
          RAL
          ADD C
          INX H
          ADD M
          STAX D
          RET
TIMING:   PUSH D
          PUSH B
          MVI B,01H
Z3:       MVI C,03H
Z2:       MVI D,0FFH
Z1:       MVI E,0FFH
Z0:       DCR E
          JNZ Z0
          DCR D
          JNZ Z1
          DCR C
          JNZ Z2
          DCR B
          JNZ Z3
          POP B
          POP D
          RET
          ORG 0700H
          DB 12H,00H
          ORG 07A0H
          DB 54H,41H,52H,49H,48H,20H,20H,20H
          DB 50H,4CH,41H,4BH,41H,20H,20H,20H
```

```
DB 54H,41H,52H,54H,49H,4DH,0BH,0BH
ORG 1000H
DB 00H,00H,39H,5EH,79H,71H,00H,00H
DB 00H,00H,7FH,6FH,77H,7CH,00H,00H
DB 00H,00H,66H,6DH,7DH,07H,00H,00H
DB 00H,00H,3FH,06H,5BH,4FH,00H,00H
ORG 1100H
DB 3FH,06H,5BH,4FH,66H,6DH,7DH,07H
DB 7FH,6FH,77H,7CH,39H,5EH,79H,71H
ORG 1200H
DB 00H,00H,0CH,0DH,0EH,0FH,00H,00H
DB 00H,00H,08H,09H,0AH,0BH,00H,00H
DB 00H,00H,04H,05H,06H,07H,00H,00H
DB 00H,00H,00H,01H,02H,03H,00H,00H
END
```

EK-2

intel®

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64k Bytes of Memory

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

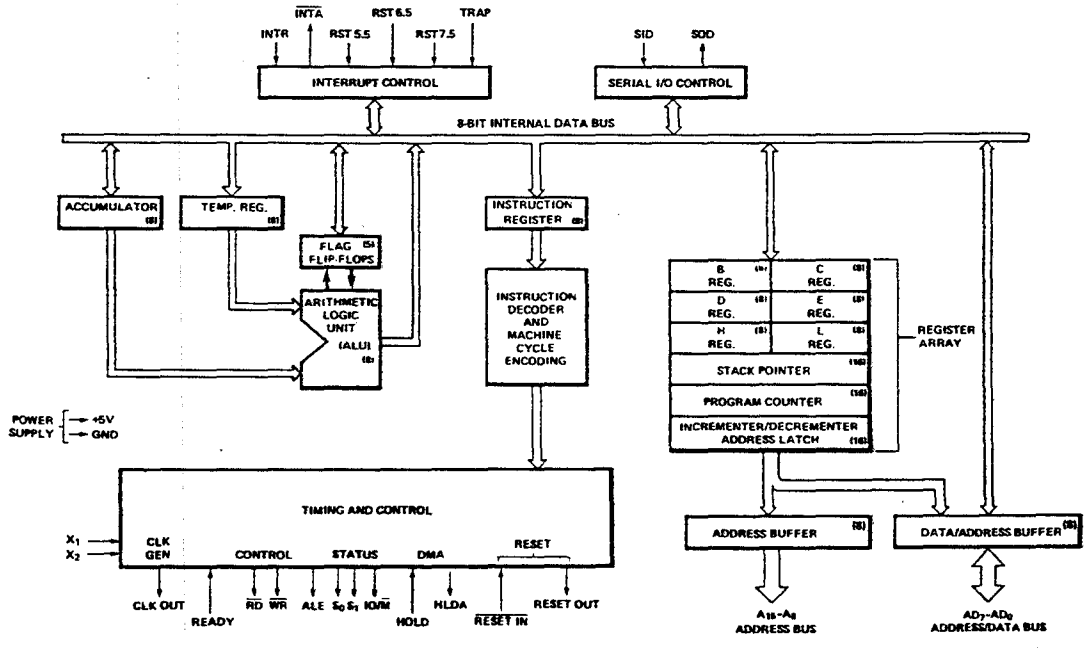


Figure 1. 8085A CPU Functional Block Diagram

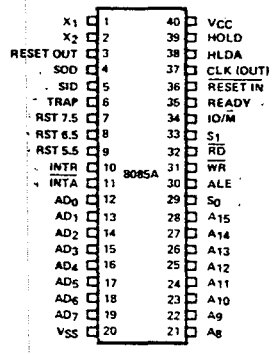


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol — **Function**

A_8–A_{15} (Output, 3-state)
Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD_{0-7} (Input/Output, 3-state)
Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)
Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1, and IO/$\overline{M}$ (Output)
Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)
X = unspecified

Symbol — **Function**

S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

$\overline{RD}$ (Output, 3-state)
READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET.

$\overline{WR}$ (Output, 3-state)
WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.

READY (Input)
If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.

HOLD (Input)
HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)
HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

INTR (Input)
INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

MCS-80/85

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. (See Section 5.2.7.) The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. See SIM, Chapter 5.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the 8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

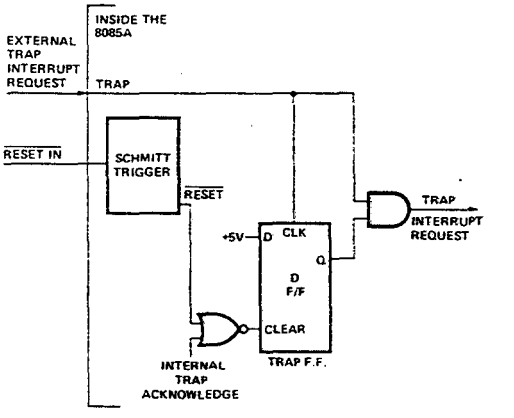


Figure 3. TRAP and $\overline{RESET\ IN}$ Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled. See the description of the RIM instruction in Chapter 5.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085A or 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) ≤ 30 pf
C_S (shunt capacitance) ≤ 7 pf
R_S (equivalent shunt resistance ≤ 75 Ohms
Drive level: 10 mW
Frequency tolerance: ±.005% suggested)

Note the use of the 20pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085A, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

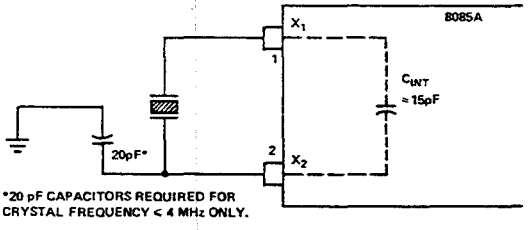
$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

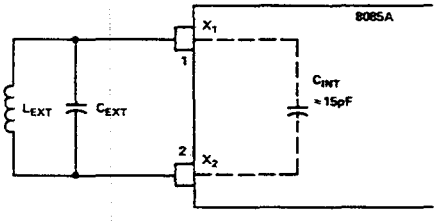
Figure 4 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4 V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figue 4D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 4E). To prevent self-oscillation of the 8085A, be sure that X_2 is not coupled back to X_1 through the driving circuit.

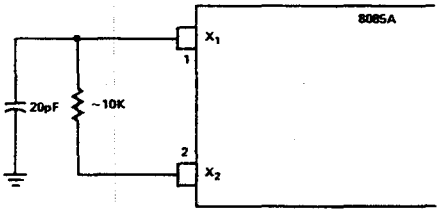


*20 pF CAPACITORS REQUIRED FOR CRYSTAL FREQUENCY < 4 MHz ONLY.

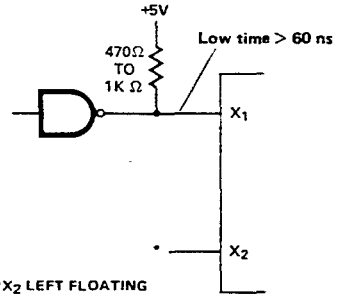
A. Quartz Crystal Clock Driver



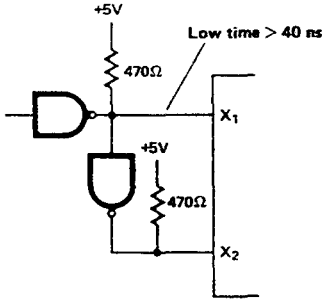
B. LC Tuned Circuit Clock Driver



C. RC Circuit Clock Driver



D. 1-6 MHz Input Frequency External Clock Driver Circuit



E. 1-10 MHz Input Frequency External Clock Driver Circuit

Figure 4. Clock Driver Circuits

GENERATING AN 8085A WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each 8085A machine cycle

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

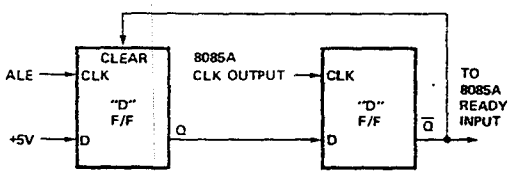


Figure 5. Generation of a Wait State for 8085A CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. HOLD causes the cpu to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085A family includes memory components, which are directly compatible to the 8085A cpu. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using 8085A.

The 8085A cpu can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 8.

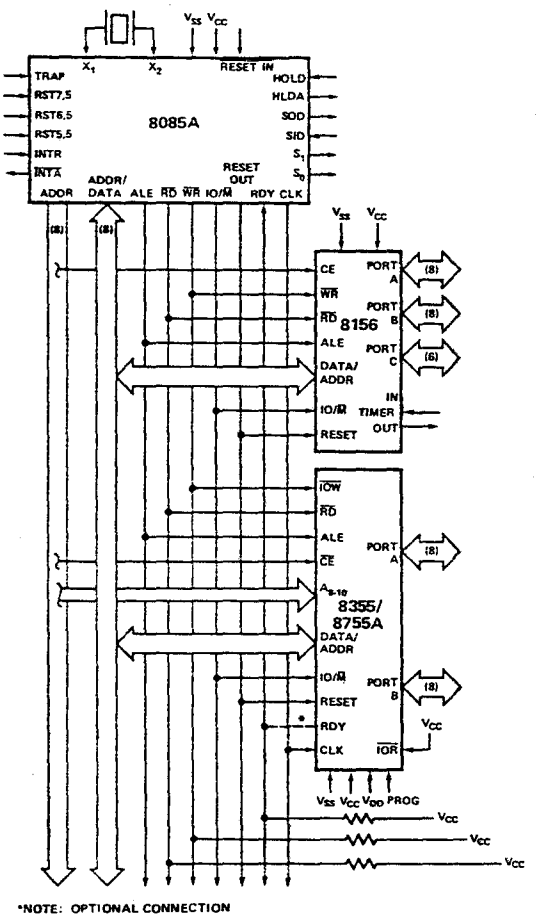


Figure 6. 8085A Minimum System (Standard I/O Technique)

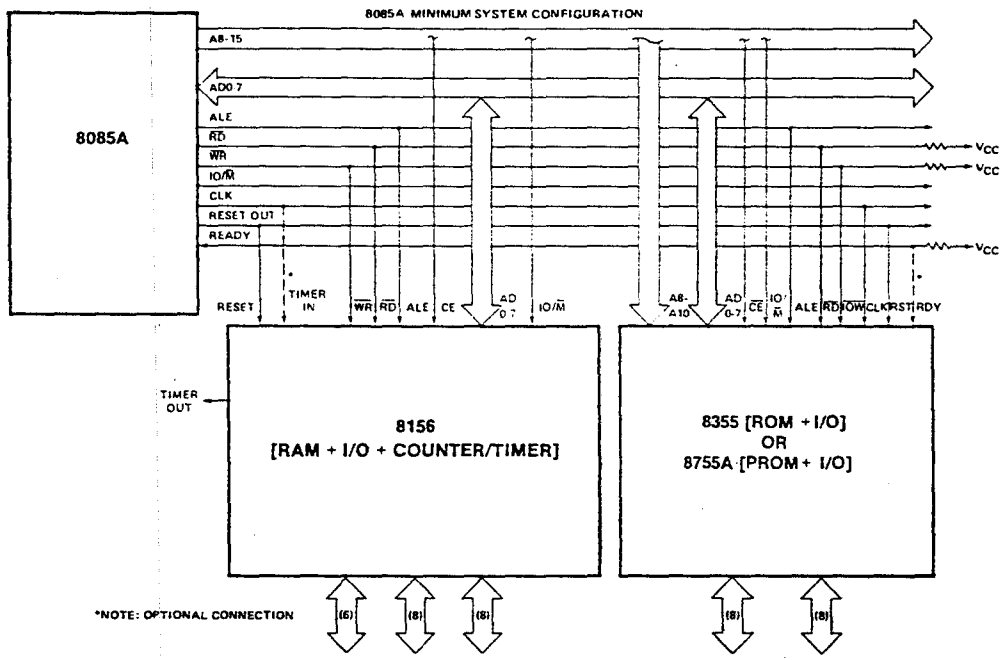


Figure 7. MCS-85™ Minimum System (Memory Mapped I/O)

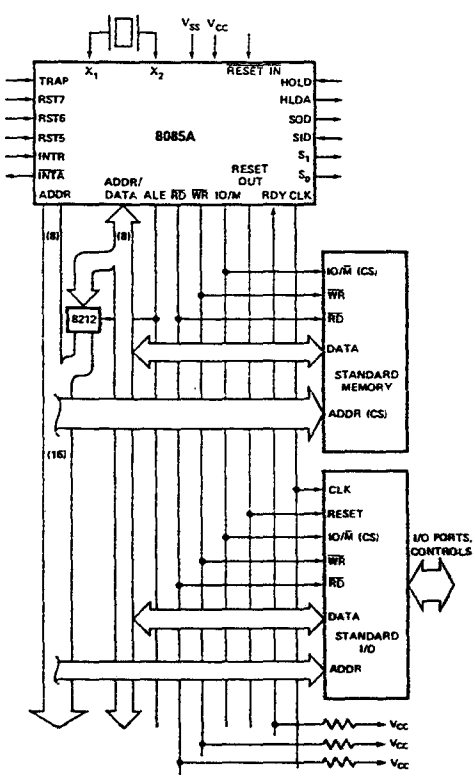


Figure 8. MCS-85™ System (Using Standard Memories)

BASIC SYSTEM TIMING

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. 8085A MACHINE CYCLE CHART

MACHINE CYCLE			STATUS			CONTROL		
			$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK. OF RST,TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

TABLE 3. 8085A MACHINE STATE CHART

Machine State	Status & Buses				Control		
	S1,S0	$IO/\overline{M}$	A_8–A_{15}	AD_0–AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4–T_6 of INA machine cycle.

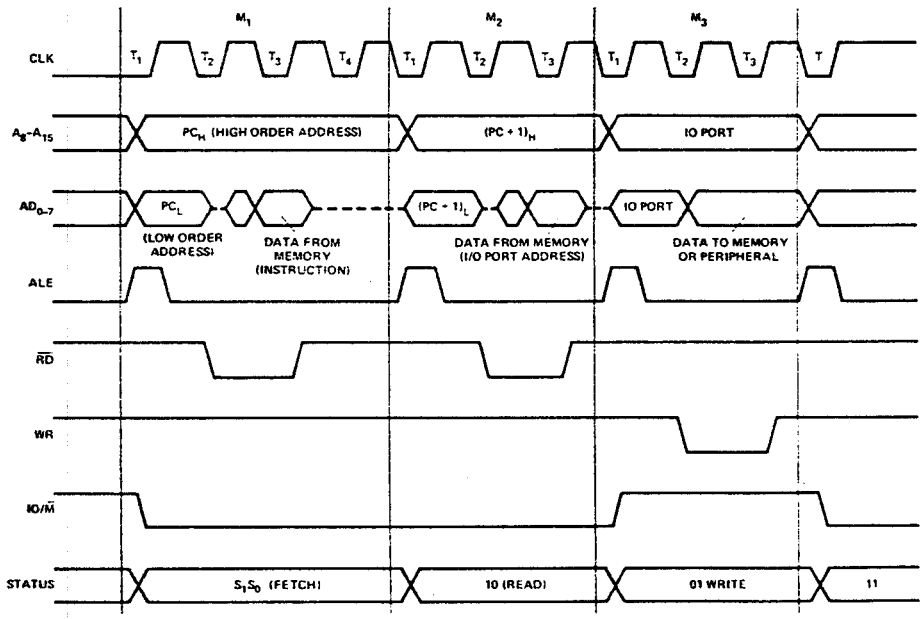


Figure 9. 8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 5. D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 6. A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	8085A[2]		8085A-2[2]		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE[1]	115		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE Low During CLK High	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns

Table 6. A.C. Characteristics (Cont.)

Symbol	Parameter	8085A[2]		8085A-2[2]		Units
		Min.	Max.	Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$[7]	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes:
1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 150 pF.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output votage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 7.
7. Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

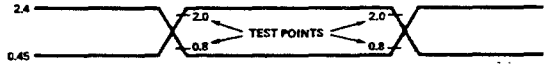


TABLE 7. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

8085A

t_{AL}	–	(1/2) T - 45	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 180	MAX

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

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t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 50	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 50	MIN
t_{LC}	–	(1/2) T - 40	MIN
t_{AD}	–	(5/2 + N) T - 150	MAX
t_{RD}	–	(3/2 + N) T - 150	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 70	MIN
t_{WD}	–	(1/2) T - 40	MIN
t_{CC}	–	(3/2 + N) T - 70	MIN
t_{CL}	–	(1/2) T - 75	MIN
t_{ARY}	–	(3/2) T - 200	MAX
t_{HACK}	–	(1/2) T - 60	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 85	MIN
t_1	–	(1/2) T - 60	MIN
t_2	–	(1/2) T - 30	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 130	MAX

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

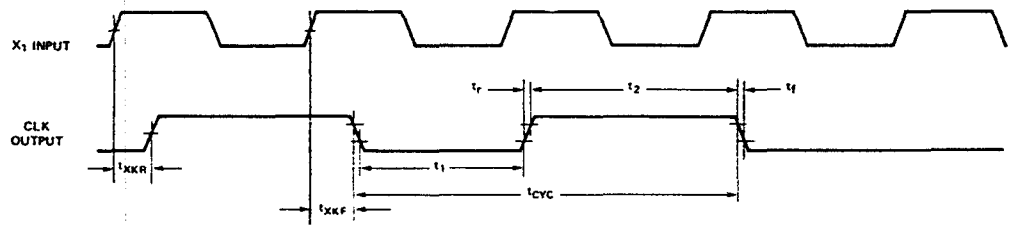
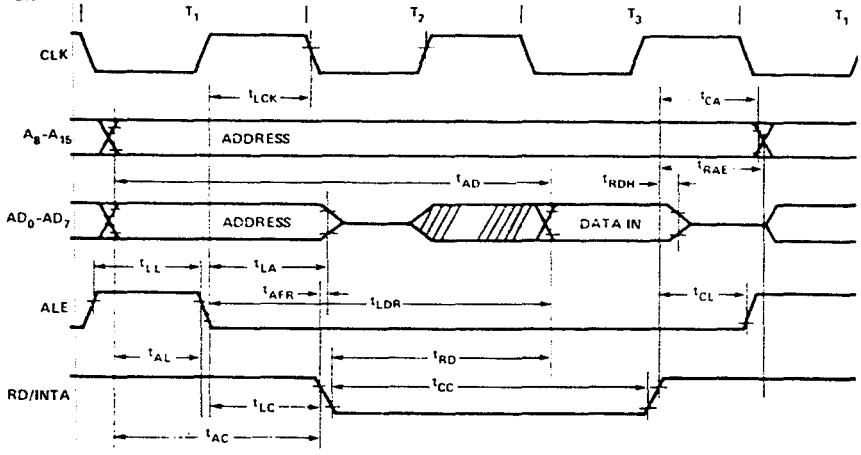
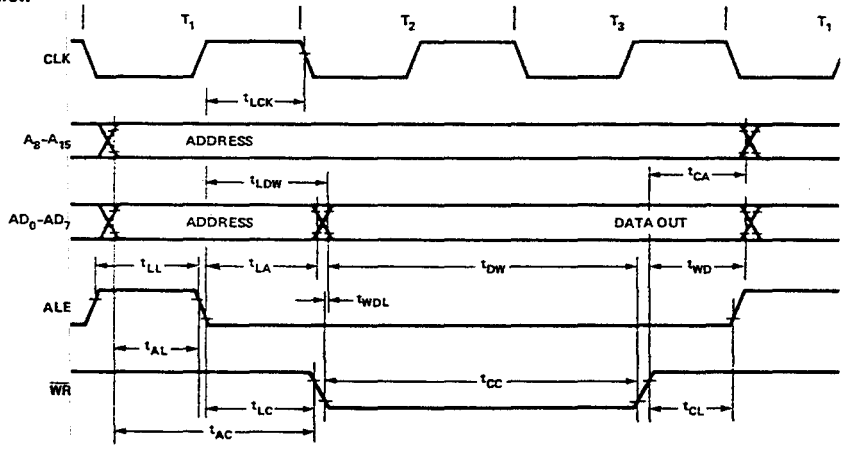


Figure 10. Clock Timing Waveform

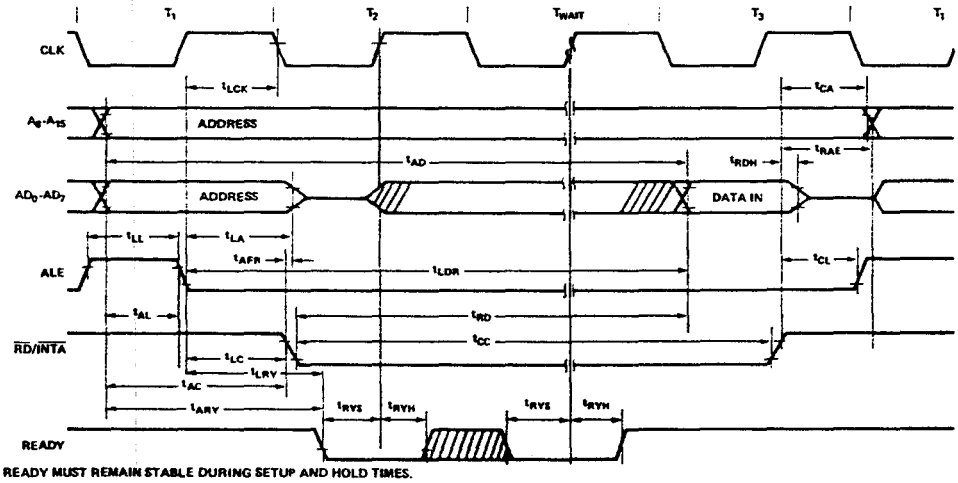
Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.



NOTE 1: READY MUST REMAIN STABLE DURING SETUP AND HOLD TIMES.

Figure 11. 8085A Bus Timing, With and Without Wait

Hold Operation

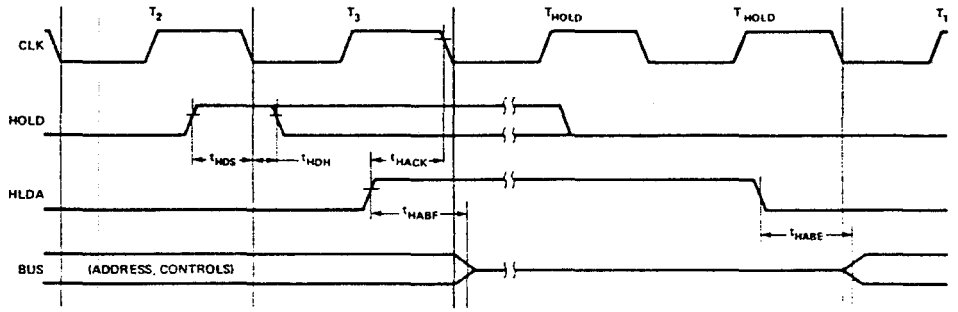


Figure 12. 8085A Hold Timing.

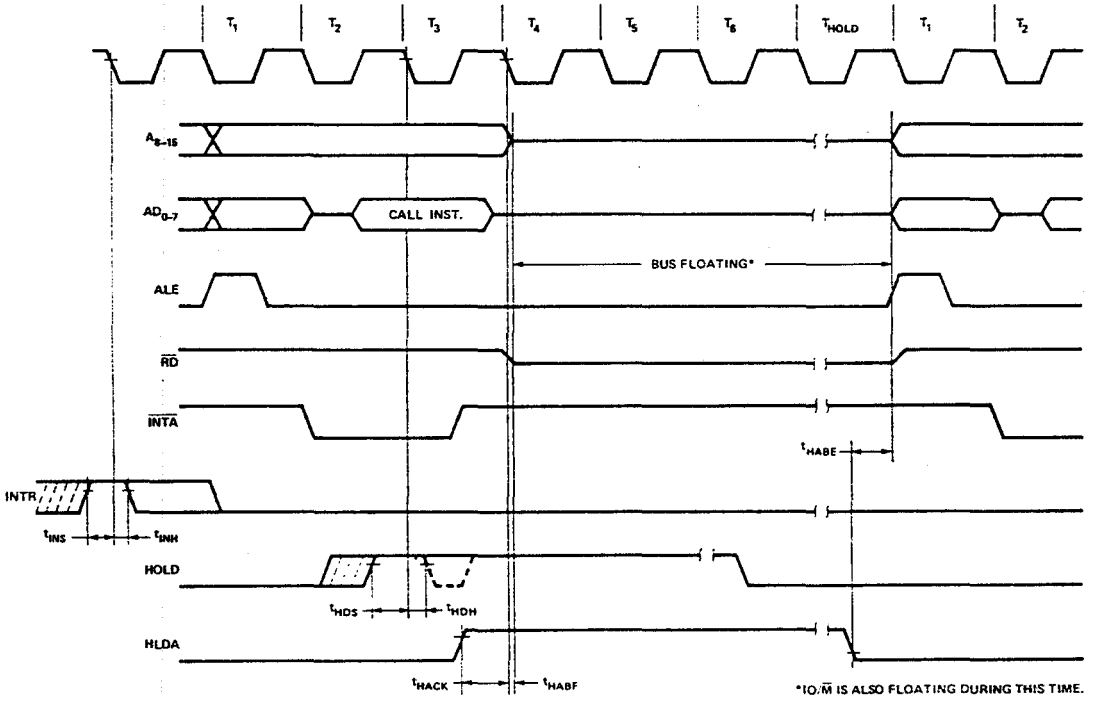


Figure 13. 8085A Interrupt and Hold Timing

8085A INSTRUCTION SET SUMMARY BY FUNCTIONAL GROUPING

Table 6-1

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
MOVE, LOAD, AND STORE									
MOV r1 r2	Move register to register	0	1	D	D	D	S	S	S
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0
MVI r	Move immediate register	0	0	D	D	D	1	1	0
MVI M	Move immediate memory	0	0	1	1	0	1	1	0
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1
STAX B	Store A indirect	0	0	0	0	0	0	1	0
STAX D	Store A indirect	0	0	0	1	0	0	1	0
LDAX B	Load A indirect	0	0	0	0	1	0	1	0
LDAX D	Load A indirect	0	0	0	1	1	0	1	0
STA	Store A direct	0	0	1	1	0	0	1	0
LDA	Load A direct	0	0	1	1	1	0	1	0
SHLD	Store H & L direct	0	0	1	0	0	0	1	0
LHLD	Load H & L direct	0	0	1	0	1	0	1	0
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1
STACK OPS									
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1
JUMP									
JMP	Jump unconditional	1	1	0	0	0	0	1	1
JC	Jump on carry	1	1	0	1	1	0	1	0
JNC	Jump on no carry	1	1	0	1	0	0	1	0
JZ	Jump on zero	1	1	0	0	1	0	1	0
JNZ	Jump on no zero	1	1	0	0	0	0	1	0
JP	Jump on positive	1	1	1	1	0	0	1	0
JM	Jump on minus	1	1	1	1	1	0	1	0
JPE	Jump on parity even	1	1	1	0	1	0	1	0
JPO	Jump on parity odd	1	1	1	0	0	0	1	0
PCHL	H & L to program counter	1	1	1	0	1	0	0	1
CALL									
CALL	Call unconditional	1	1	0	0	1	1	0	1
CC	Call on carry	1	1	0	1	1	1	0	0
CNC	Call on no carry	1	1	0	1	0	1	0	0
CZ	Call on zero	1	1	0	0	1	1	0	0
CNZ	Call on no zero	1	1	0	0	0	1	0	0
CP	Call on positive	1	1	1	1	0	1	0	0
CM	Call on minus	1	1	1	1	1	1	0	0
CPE	Call on parity even	1	1	1	0	1	1	0	0
CPO	Call on parity odd	1	1	1	0	0	1	0	0
RETURN									
RET	Return	1	1	0	0	1	0	0	1
RC	Return on carry	1	1	0	1	1	0	0	0
RNC	Return on no carry	1	1	0	1	0	0	0	0
RZ	Return on zero	1	1	0	0	1	0	0	0
RNZ	Return on no zero	1	1	0	0	0	0	0	0
RP	Return on positive	1	1	1	1	0	0	0	0
RM	Return on minus	1	1	1	1	1	0	0	0
RPE	Return on parity even	1	1	1	0	1	0	0	0
RPO	Return on parity odd	1	1	1	0	0	0	0	0
RESTART									
RST	Restart	1	1	A	A	A	1	1	1
INPUT/OUTPUT									
IN	Input	1	1	0	1	1	0	1	1
OUT	Output	1	1	0	1	0	0	1	1
INCREMENT AND DECREMENT									
INR r	Increment register	0	0	D	D	D	1	0	0
DCR r	Decrement register	0	0	D	D	D	1	0	1
INR M	Increment memory	0	0	1	1	0	1	0	0
DCR M	Decrement memory	0	0	1	1	0	1	0	1
INX B	Increment B & C registers	0	0	0	0	0	0	1	1
INX D	Increment D & E registers	0	0	0	1	0	0	1	1
INX H	Increment H & L registers	0	0	1	0	0	0	1	1
DCX B	Decrement B & C	0	0	0	0	1	0	1	1
DCX D	Decrement D & E	0	0	0	1	1	0	1	1
DCX H	Decrement H & L	0	0	1	0	1	0	1	1
ADD									
ADD r	Add register to A	1	0	0	0	0	S	S	S
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S
ADD M	Add memory to A	1	0	0	0	0	1	1	0
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0
ADI	Add immediate to A	1	1	0	0	0	1	1	0
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1
SUBTRACT									
SUB r	Subtract register from A	1	0	0	1	0	S	S	S
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0

8085A INSTRUCTION SET SUMMARY (Cont'd)

Table 6-1

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0
LOGICAL									
ANA r	And register with A	1	0	1	0	0	S	S	S
XRA r	Exclusive OR register with A	1	0	1	0	1	S	S	S
ORA r	OR register with A	1	0	1	1	0	S	S	S
CMP r	Compare register with A	1	0	1	1	1	S	S	S
ANA M	And memory with A	1	0	1	0	0	1	1	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0
ANI	And immediate with A	1	1	1	0	0	1	1	0
XRI	Exclusive OR immediate with A	1	1	1	0	1	1	1	0
ORI	OR immediate with A	1	1	1	1	0	1	1	0
CPI	Compare immediate with A	1	1	1	1	1	1	1	0
ROTATE									
RLC	Rotate A left	0	0	0	0	0	1	1	1
RRC	Rotate A right	0	0	0	0	1	1	1	1
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1
SPECIALS									
CMA	Complement A	0	0	1	0	1	1	1	1
STC	Set carry	0	0	1	1	0	1	1	1
CMC	Complement carry	0	0	1	1	1	1	1	1
DAA	Decimal adjust A	0	0	1	0	0	1	1	1
CONTROL									
EI	Enable Interrupts	1	1	1	1	1	0	1	1
DI	Disable Interrupt	1	1	1	1	0	0	1	1
NOP	No-operation	0	0	0	0	0	0	0	0
HLT	Halt	0	1	1	1	0	1	1	0
NEW 8085A INSTRUCTIONS									
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0

NOTES: 1. DDS or SSS: B 000, C 001, D 010, E011, H 100, L 101, Memory 110, A 111.

2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

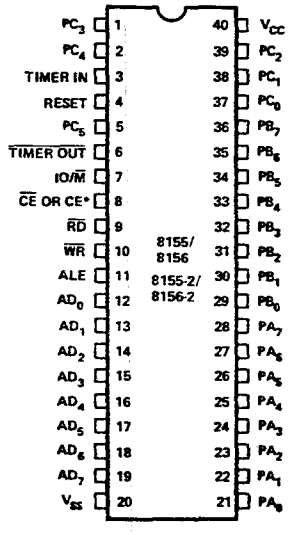
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

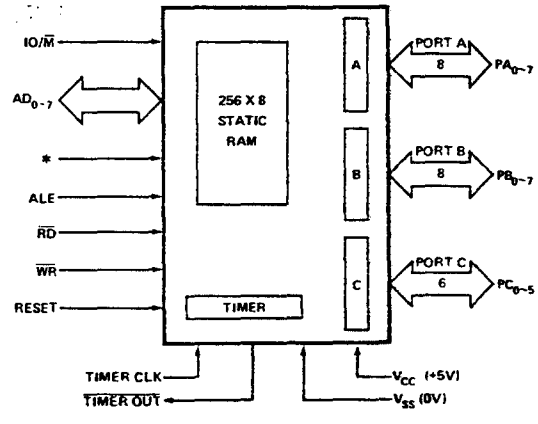
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: 8155/8155-2 = $\overline{CE}$, 8156/8156-2 = CE

8155/8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input/output)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — ABF (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

DESCRIPTION

The 8155/8156 contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion. (See Figure 1.)

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE. (See Figure 2.)

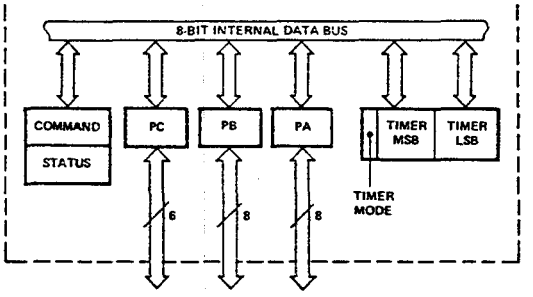
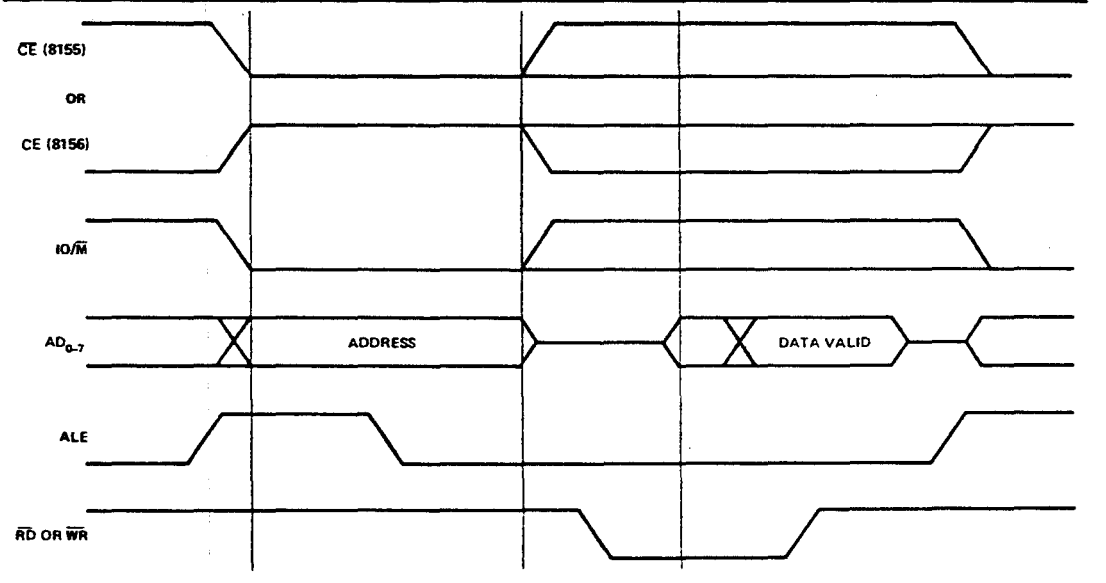


Figure 1. 8155/8156 Internal Registers



NOTE: FOR DETAILED TIMING INFORMATION, SEE FIGURE 12 AND A.C. CHARACTERISTICS.

Figure 2. 8155/8156 On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 3. The contents of the command register may never be read.

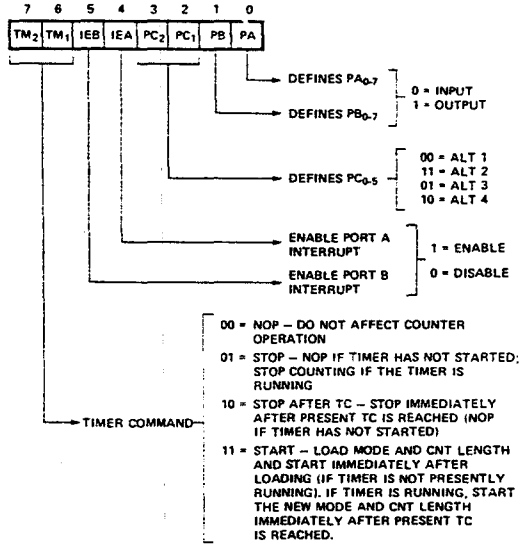


Figure 3. Command Register Bit Assignment

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 4. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

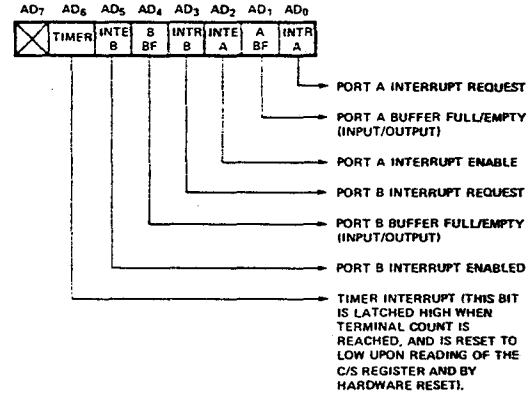


Figure 4. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155/8156 consists of five registers: (See Figure 5.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C — General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care

† I/O Address must be qualified by CE = 1 (8156 or $\overline{CE}$ = 0 (8155 and IO/$\overline{M}$ = 1 in order to select the appropriate register.

Figure 5. I/O port and Timer Addressing Scheme

Figure 6 shows how I/O PORTS A and B are structured within the 8155 and 8156:

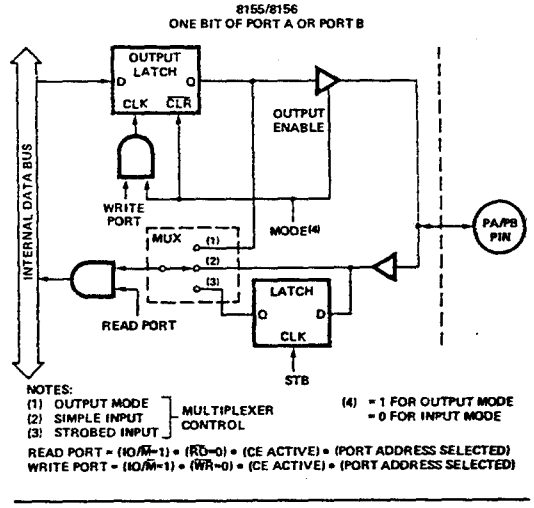


Figure 6. 8155/8156 Port Functions

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155/8156 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155/56 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 7 shows how the 8155/8156 I/O ports might be configured in a typical MCS-85 system.

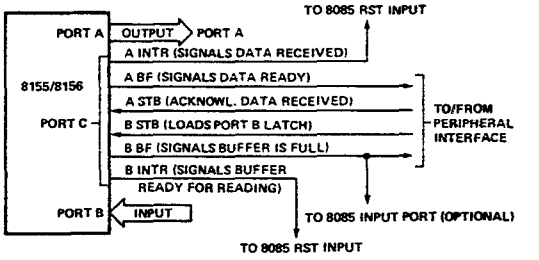


Figure 7. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 5).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 8). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

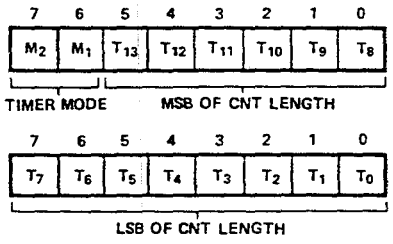


Figure 8. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

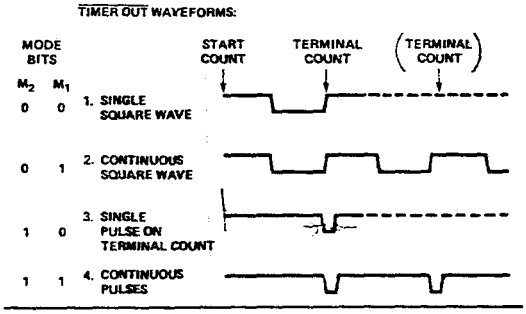


Figure 9. Timer Modes

Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 10.

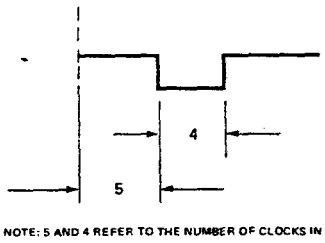


Figure 10. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155/8156 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155/56 always counts out the right number of pulses in generating the TIMER OUT waveforms.

EXAMPLE PROGRAM

Following is an actual sequence of program steps that adjusts the 8155/56 count register contents to obtain the count, extracted from Intel® Application Note AP38. "Application Techniques for the Intel 8085A Bus." First store the value of the full original count in register HL of the 8085A. Then stop the count to avoid getting an incorrect count value. Then sample the timer-counter, storing the lower-order byte of the current count register in register C and the higher-order count byte in register B. Then, call the following 8080A/8085A subroutine:

```
ADJUST, 78      MOV A,B     ;Load accumulator with upper half
                            ; of count.
        E63F    ANI 3F      ;Reset upper 2 bits and clear carry.
        1F      RAR         ;Rotate right through carry.
        47      MOV B,A     ;Store shifted value back in B.
        79      MOV A,C     ;Load accumulator with lower half.
        1F      RAR         ;Rotate right through carry.
        4F      MOV C,A     ;Store lower byte in C.
        DØ      RNC         ;If in 2nd half of count, return.
                            ;If in 1st half, go on.
        3F      CMC         ;Clear carry.
        7C      MOV A,H     ;Divide full count by 2. (If HL
                            ;is odd, disregard remainder.)
        1F      RAR
        67      MOV H,A
        7D      MOV A,L
        1F      RAR
        6F      MOV L,A
        09      DAD B       ;Double-precision add HL and BC.
        44      MOV B,H     ;Store results back in BC.
        4D      MOV C,L
        C9      RET         ;Return.
```

After executing the subroutine, BC will contain the remaining count in the current count cycle.

8085A MINIMUM SYSTEM CONFIGURATION

Figure 11a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

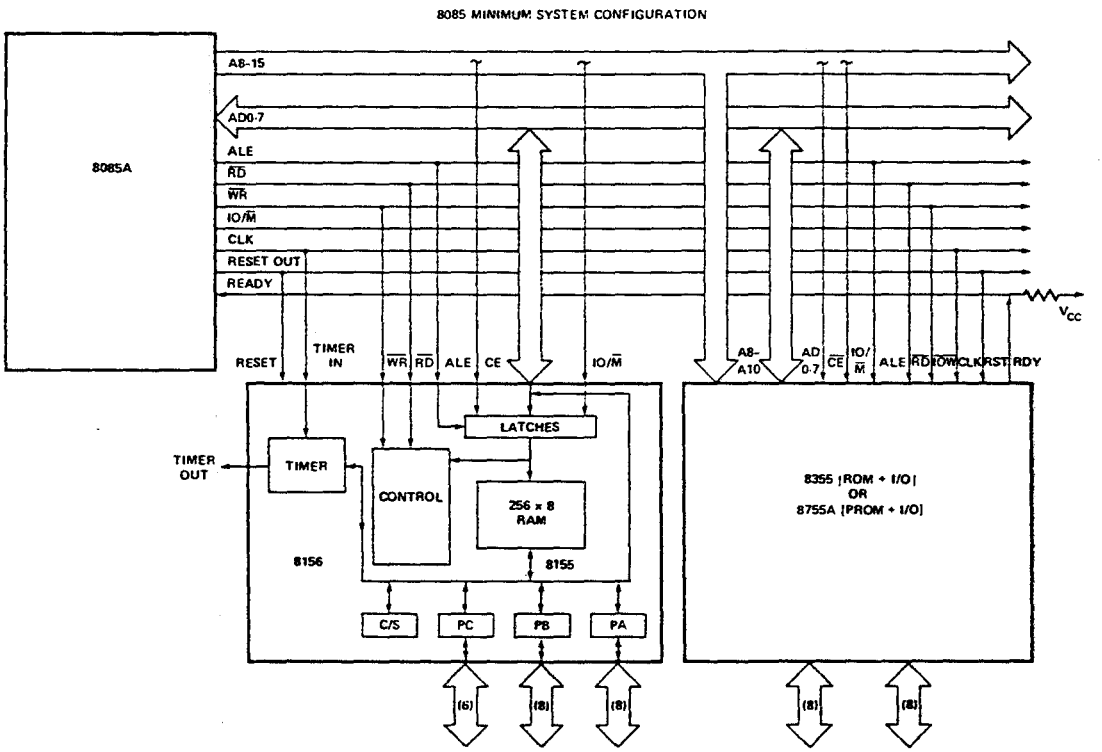


Figure 11a. 8085A Minimum System Configuration. (Memory Mapped I/O)

8088 FIVE CHIP SYSTEM

Figure 11b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

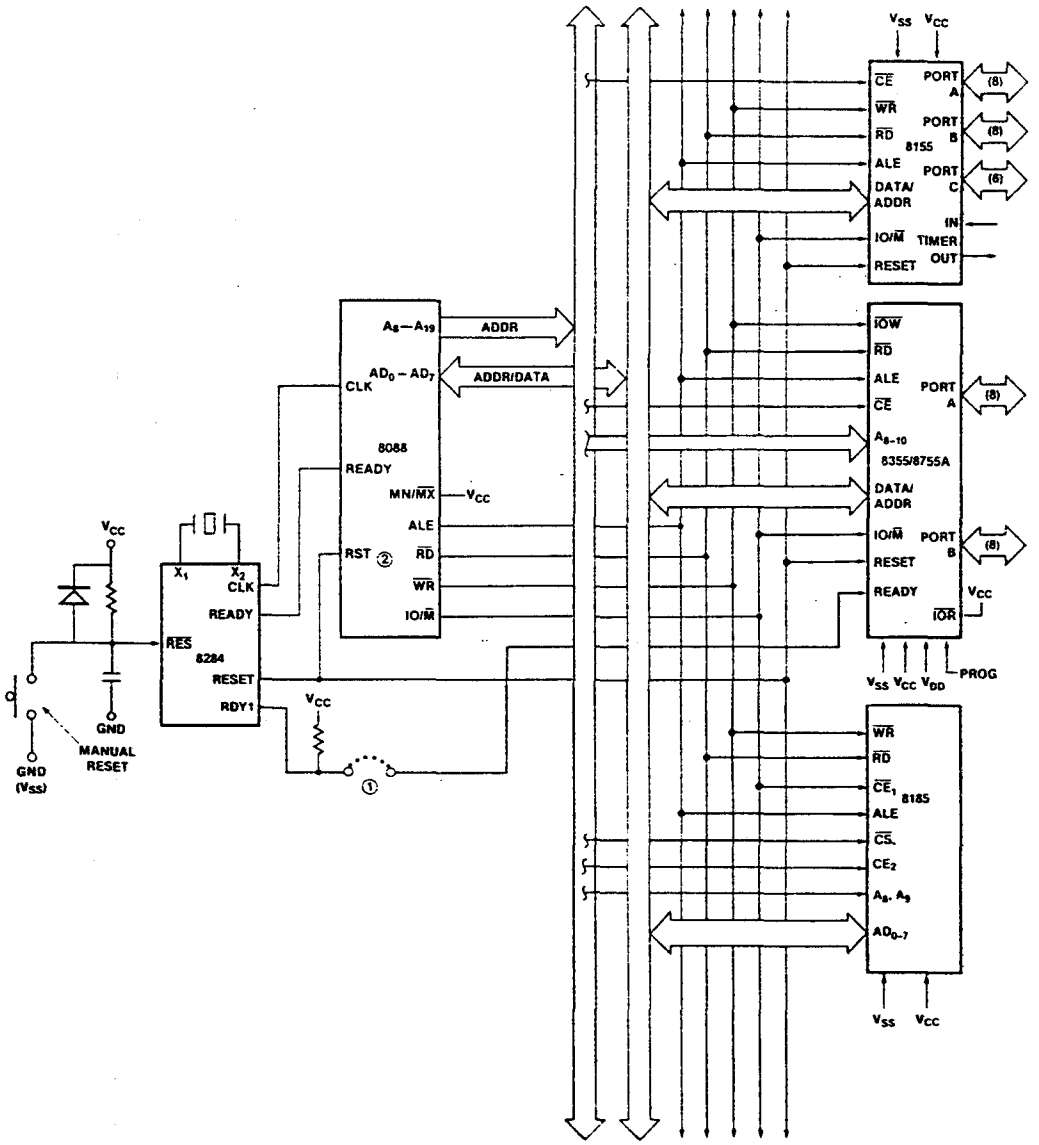


Figure 11b. 8088 Five Chip System Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		± 10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL}(CE)	Chip Enable Leakage 8155 8156		 +100 -100	 μA μA	V_{IN} = V_{CC} to 0V

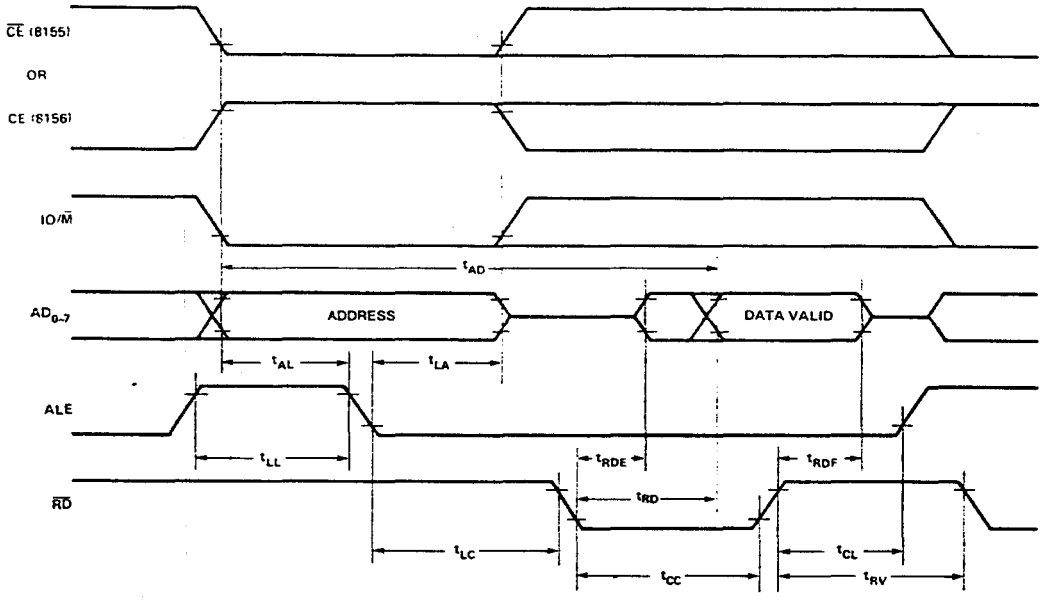
A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

		8155/8156		8155-2/8156-2 (Preliminary)		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNITS
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		100		ns
t_{WD}	Data In Hold Time After WRITE	0		0		ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns

Input Waveform for A.C. Tests:

WAVEFORMS

a. Read Cycle



b. Write Cycle

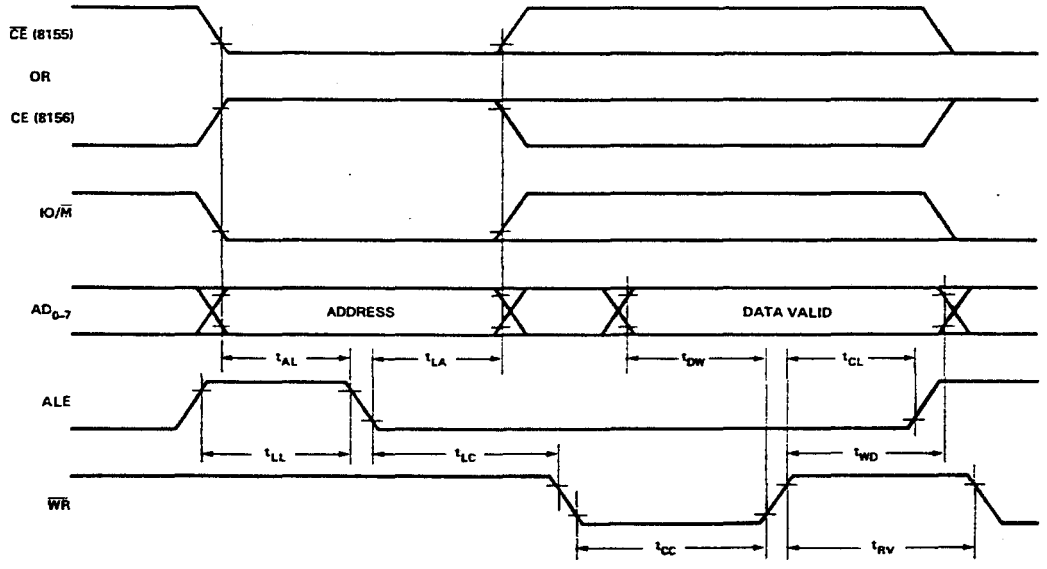
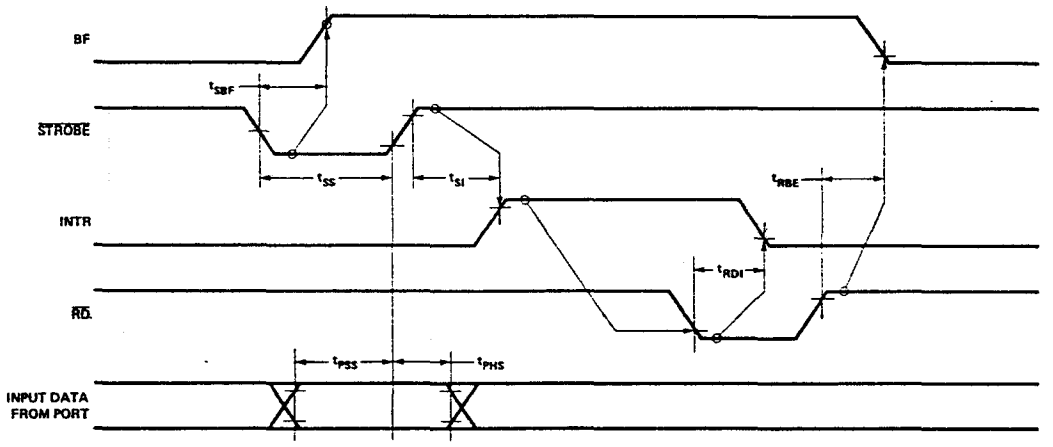


Figure 12. 8155/8156 Read/Write Timing Diagrams

a. Strobed Input Mode



b. Strobed Output Mode

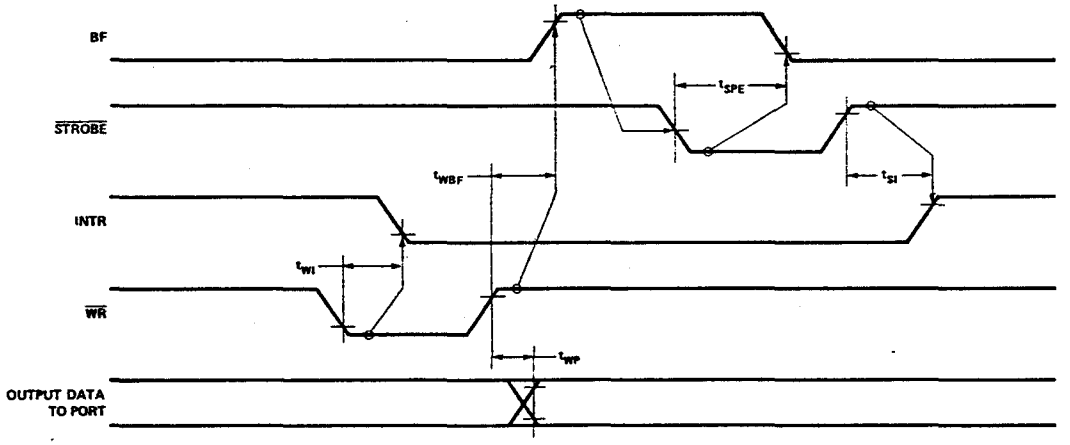
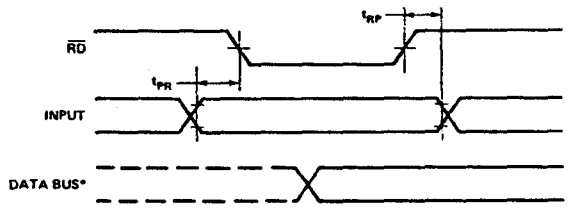
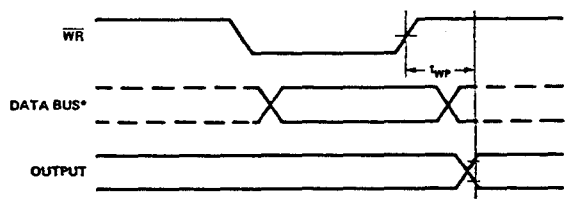


Figure 13. Strobed I/O Timing

a. Basic Input Mode

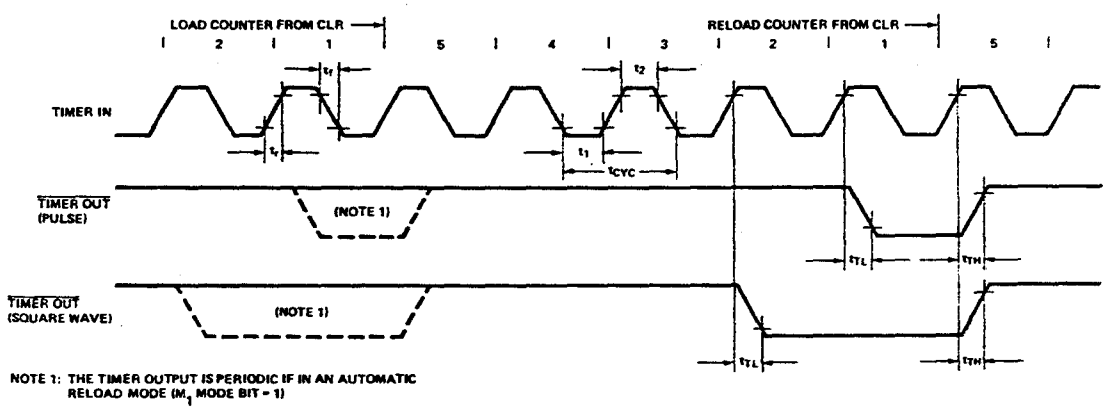


b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 14. Basic I/O Timing Waveform



NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_1 MODE BIT = 1)

Figure 15. Timer Output Waveform Countdown from 5 to 1

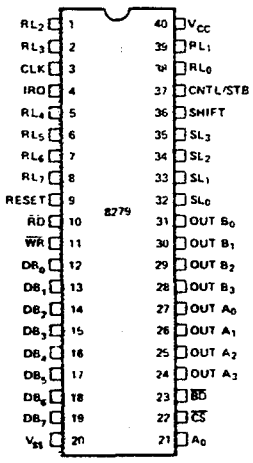
8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8-Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover with Contact Debounce
- Dual 8- or 16-Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

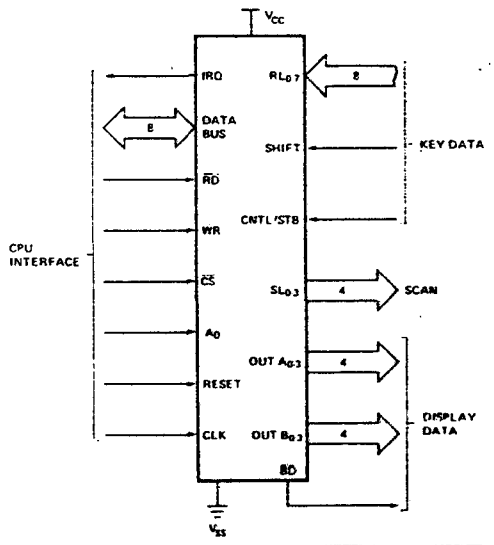
PIN CONFIGURATION



PIN NAMES

DB0-7	I/O	DATA BUS (BI-DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
CS	I	CHIP SELECT
RD	I	READ INPUT
WR	I	WRITE INPUT
A0	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL0-3	O	SCAN LINES
RL0-7	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
OUT A0-3	O	DISPLAY (A) OUTPUTS
OUT B0-3	O	DISPLAY (B) OUTPUTS
BD	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB_0-DB_7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode: 1) 16 8-bit character display —left entry. 2) Encoded scan keyboard—2 key lockout. Along with this the program clock prescaler is set to 31.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A_0	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V_{SS}, V_{CC}	Ground and power supply pins.
4	SL_0-SL_3	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL_0-RL_7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4	OUT A_0-OUT A_3	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
4	OUT B_0-OUT B_3	
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by A_0. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during $\overline{WR} \bullet \overline{CS}$ and output during $\overline{RD} \bullet \overline{CS}$.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A_0 = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

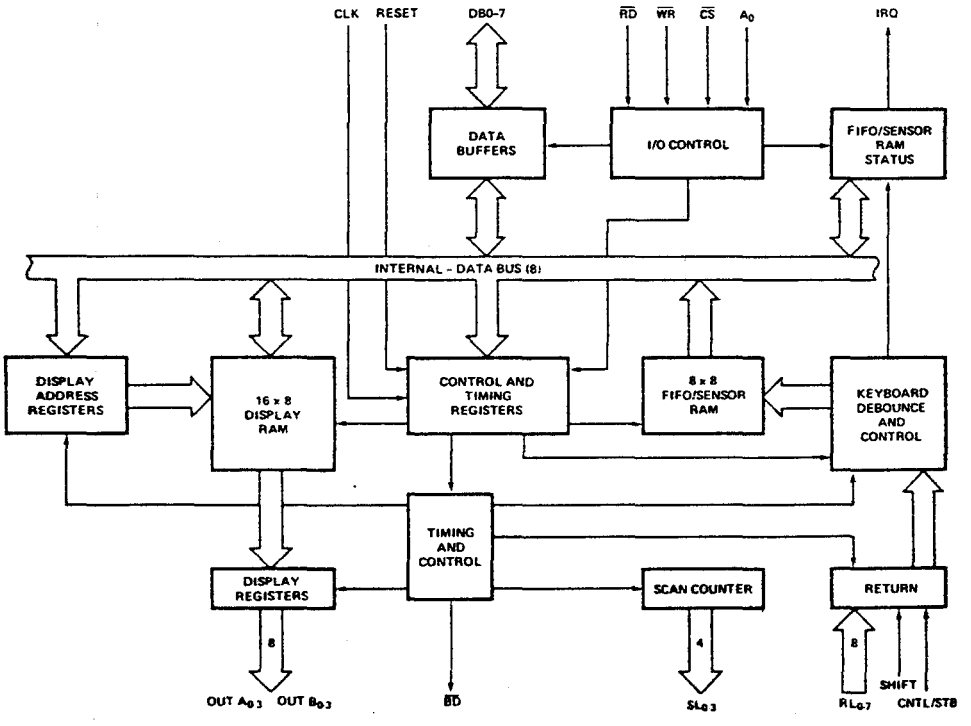
- Scanned Keyboard — with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input -- Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit ($B_0 = D_0$, $A_3 = D_7$).
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Clock Prescaler
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.



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The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

SOFTWARE OPERATION

8279 commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A_0 high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

0	0	0	Encoded Scan Keyboard — 2 Key Lockout*
0	0	1	Decoded Scan Keyboard — 2-Key Lockout
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:	0	0	1	P	P	P	P	P

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

Read FIFO/Sensor RAM

Code:	0	1	0	AI	X	A	A	A	X = Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Key-

*Default after reset.

board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

Display Write Inhibit/Blanking

Code:

				A	B	A	B
1	0	1	X	IW	IW	BL	BL

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus, and that bit A_3 corresponds to bit D_7.

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:

C_D	C_D	C_D	
0	X		All Zeros (X = Don't Care)
1	0		AB = Hex 20 (0010 0000)
1	1		All Ones
		Enable clear display when = 1 (or by C_A = 1)	

During the time the Display RAM is being cleared (~160 μs), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted ($C_F = 1$), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A, the Clear All bit, has the combined effect of C_D and C_F; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when A_0, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with A_0, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

INTERFACE CONSIDERATIONS

Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

Sensor Matrix Mode

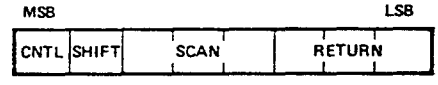
In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by (SL_{0-3} = 0) may cause multiple interrupts. (SL_0 = 0 in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

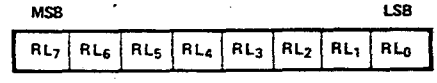
Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

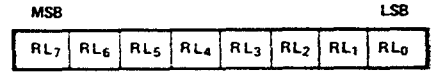


SCANNED KEYBOARD DATA FORMAT

In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.



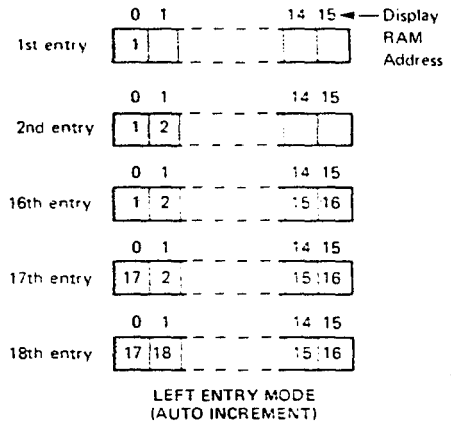
In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.



Display

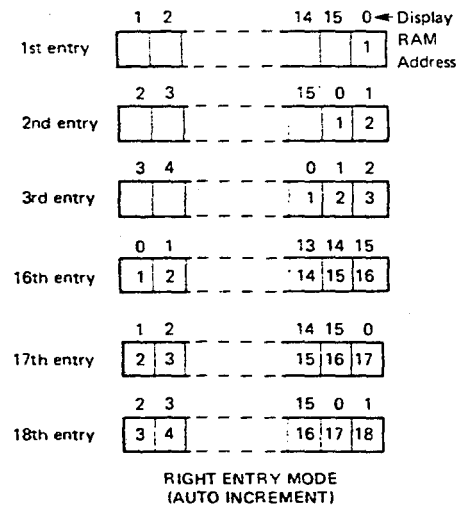
Left Entry

Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



Right Entry

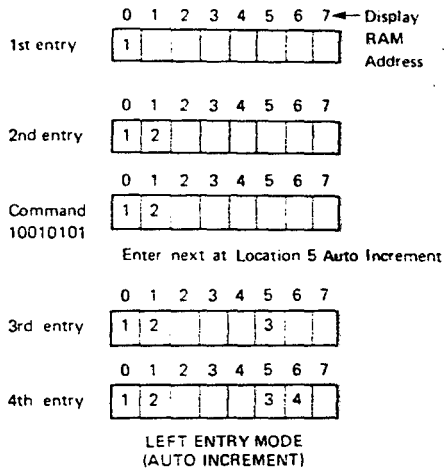
Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.



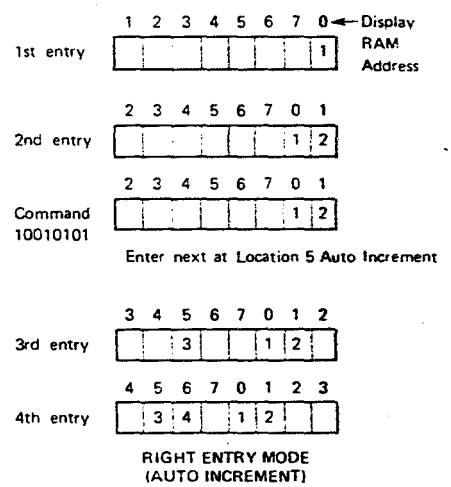
Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

Auto Increment

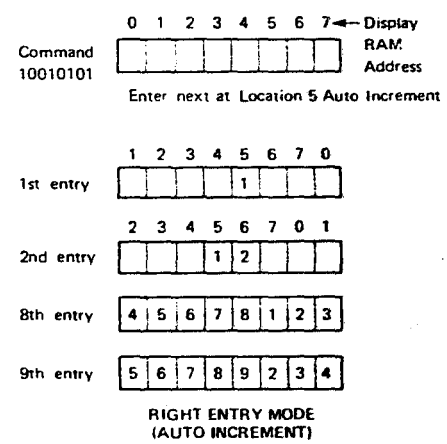
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

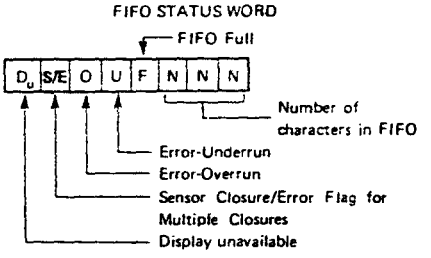
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

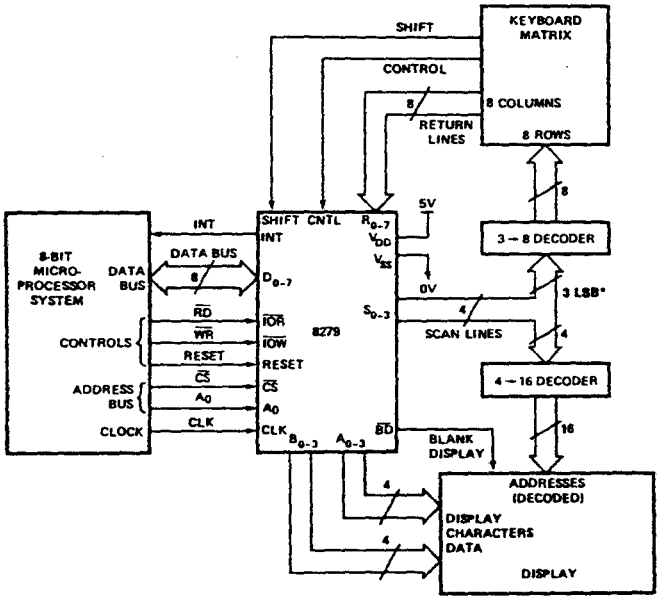
The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



APPLICATIONS



*Do not drive the keyboard decoder with the MSB of the scan lines.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to 125°C
Voltage on any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{SS} = 0V$, $V_{CC} = +5V \pm 5\%$. $V_{CC} = +5V \pm 10\%$ (8279-5)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Return Lines	-0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V_{IH1}	Input High Voltage for Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH1}	Output High Voltage on Interrupt Line	3.5		V	Note 2
V_{OH2}	Other Outputs	2.4			
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 -100	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	Power Supply Current		120	mA	

Notes:
8279, I_{OL} = 1.6mA; 8279-5, I_{OL} = 2.2mA.
8279, I_{OH} = -100μA; 8279-5, I_{OH} = -400μA.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in} = V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out} = V_{CC}$

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, (Note 1)

Bus Parameters

Read Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}[2]	Data Delay from $\overline{READ}$		300		150	ns
t_{AD}[2]	Address to Data Valid		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		0		ns
t_{WCY}	Write Cycle Time	1		1		μs

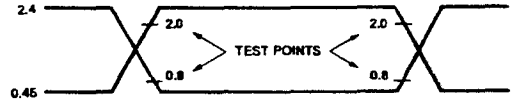
Notes:
1. 8279, V_{CC} = +5V ±5%; 8279-5, V_{CC} = +5V ±10%.
2. 8279, C_L = 100pF; 8279-5, C_L = 150pF.

Other Timings:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

Keyboard Scan Time:	5.1 msec	Digit-on Time:	480 μsec
Keyboard Debounce Time:	10.3 msec	Blanking Time:	160 μsec
Key Scan Time:	80 μsec	Internal Clock Cycle:	10 μsec
Display Scan Time:	10.3 msec		

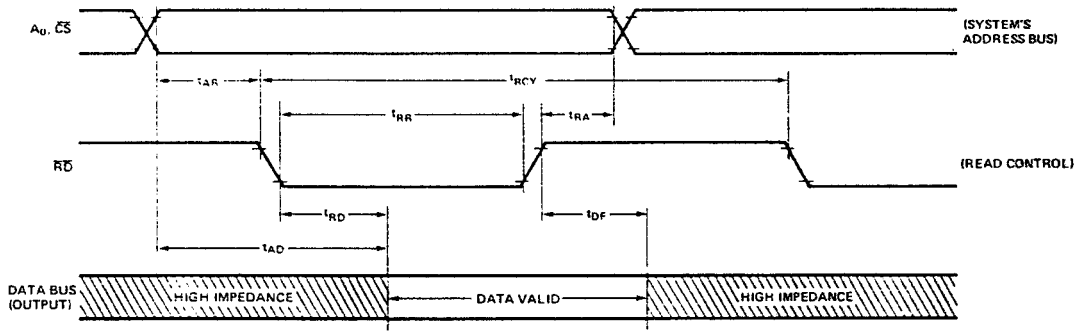
Input Waveforms For A.C. Tests



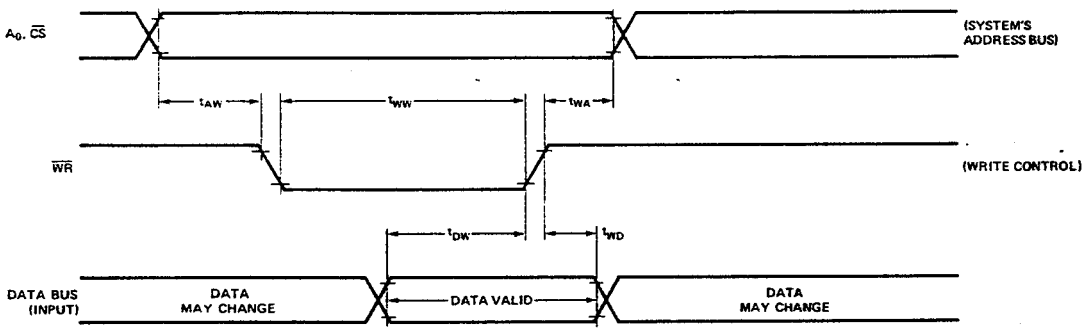
00742A

WAVEFORMS

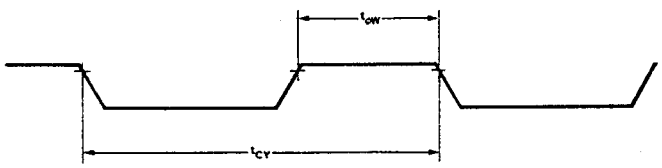
Read Operation



Write Operation



Clock Input



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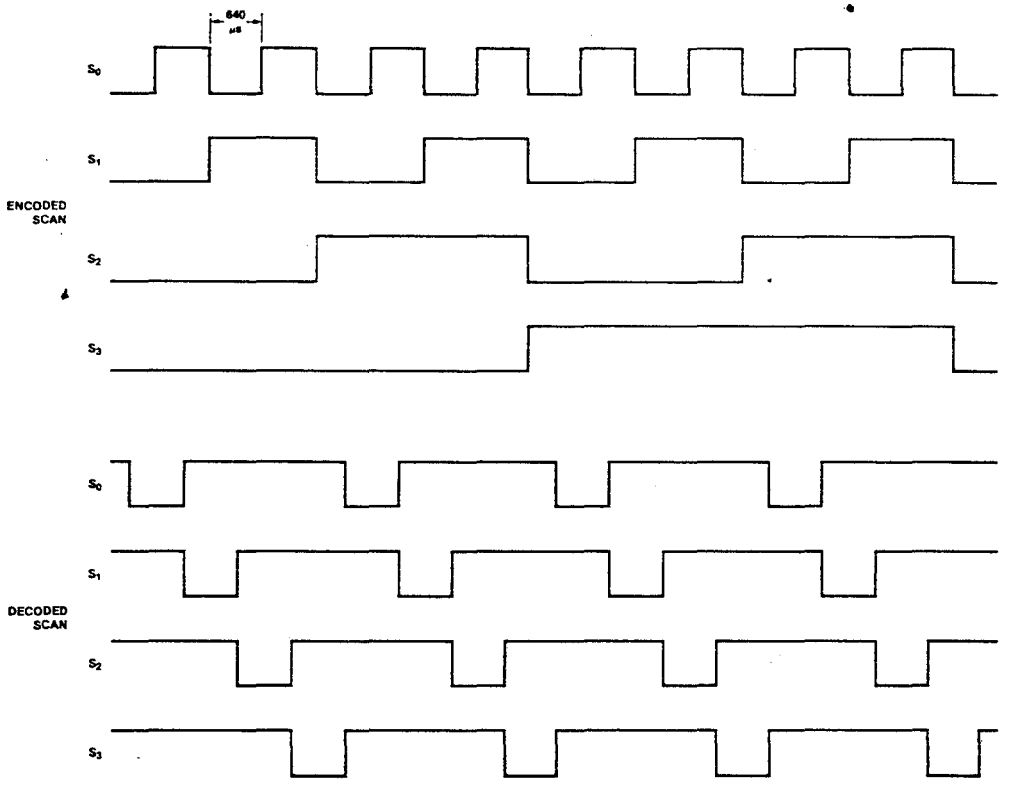
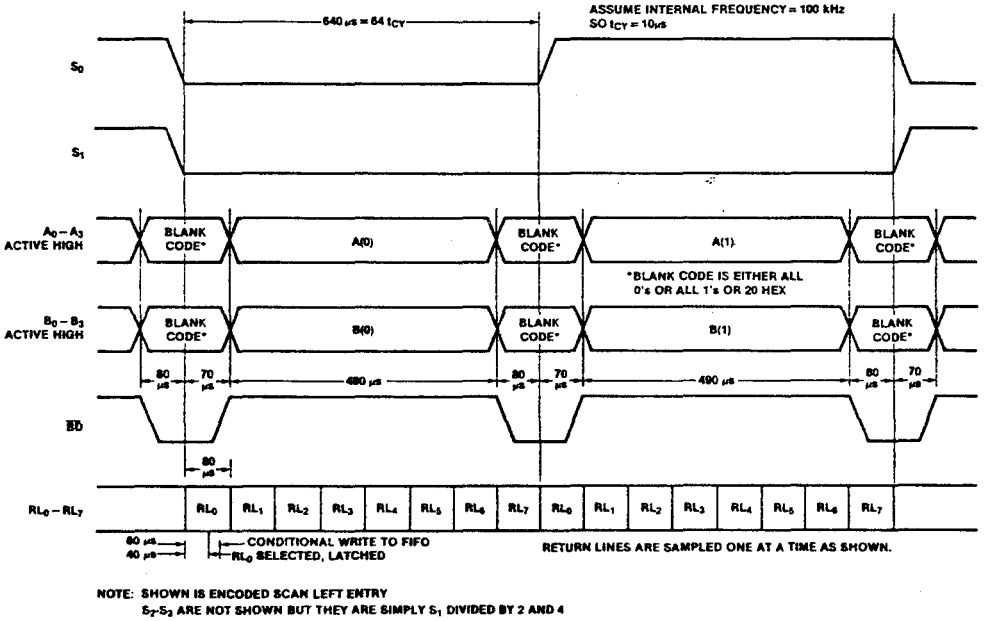
SCAN WAVEFORMS



DISPLAY WAVEFORMS



NOTE: SHOWN IS ENCODED SCAN LEFT ENTRY
S_7-S_2 ARE NOT SHOWN BUT THEY ARE SIMPLY S_1 DIVIDED BY 2 AND 4

00742A

TMS2764
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

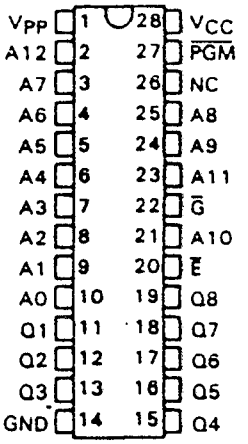
JULY 1983 – REVISED JANUARY 1984

- Organization . . . 8192 X 8
- Single +5-V Power Supply
- Pin Compatible with TMS2732A EPROM
- All Inputs and Outputs are TTL Compatible
- Performance Ranges:

	MAX ACCESS/ MIN CYCLE TIME
TMS2764-20	200 ns
TMS2764-25	250 ns
TMS2764-30	300 ns
TMS2764-35	350 ns
TMS2764-45	450 ns

- Low Active Current . . . 100 mA (Max)
- JEDEC Approved Pinout
- 21-V Power Supply Required for Programming
- Fast Programming Algorithm
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Static Operation (No Clocks, No Refresh
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or M(−55°C to 125°C) Temperature Ranges in the Future

TMS2764 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Addresses
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	outputs
V_{CC}	+5-V Power Supply
V_{PP}	+21-V Power Supply

cription

The TMS2764 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764-20 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 200 ns. This access time is compatible with high-performance microprocessors.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum active current from 100 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 600-mil dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

ation

The six modes of operation for the TMS2764 are listed in the following table.

ADVANCE INFORMATION

sheet contains information on a new product.
tions are subject to change without notice.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	X
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

V_{IL} or V_{IH}

read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 100 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to Vpp may damage the TMS2764.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on Vpp equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and Vpp = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = Vpp = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS2764's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

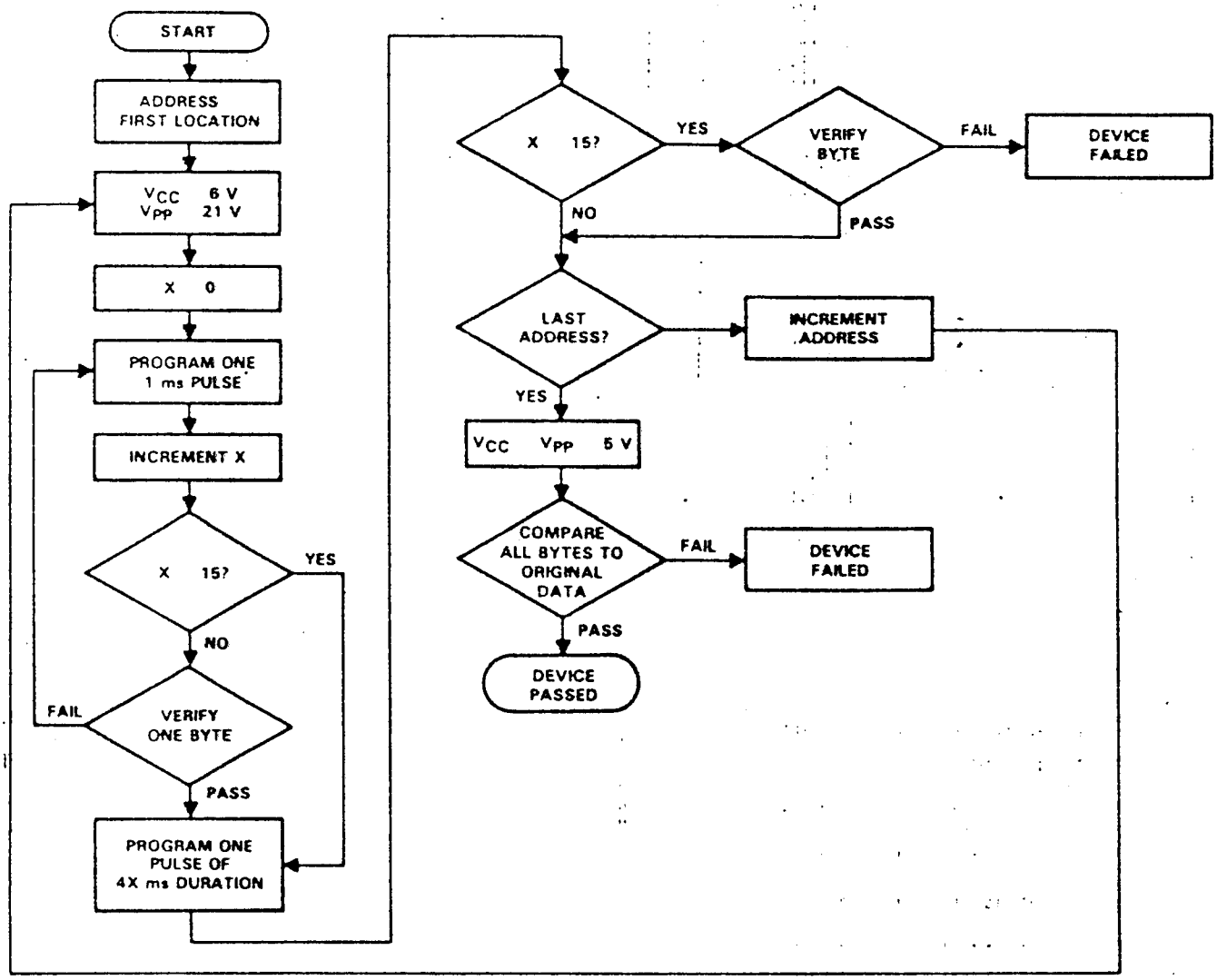


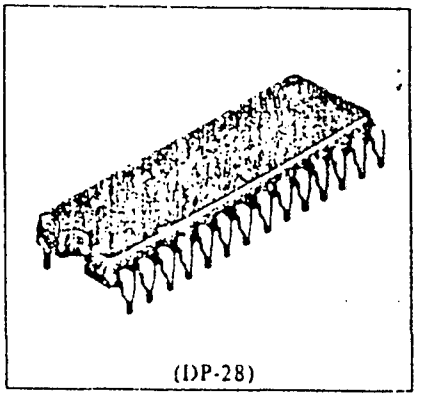
FIGURE 1 – FAST PROGRAMMING FLOWCHART

HM6264LP-10, HM6264LP-12
HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

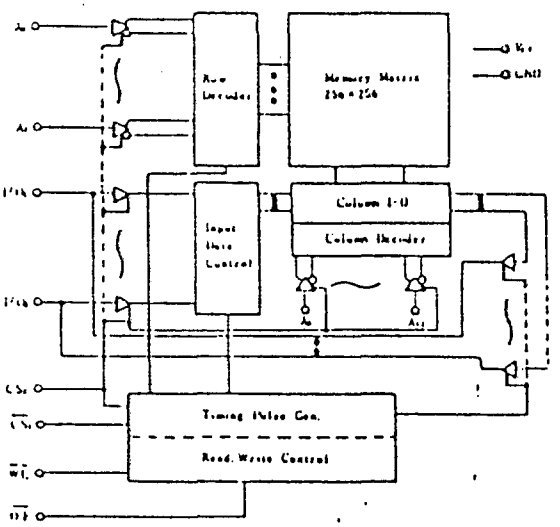
FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.01mW (typ.)
- Low Power Operation — Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

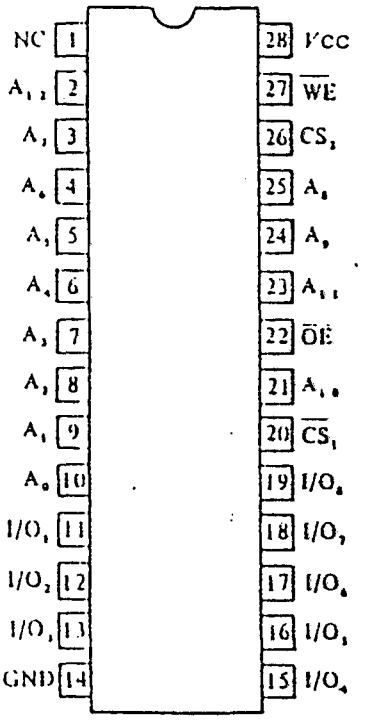


(DP-28)

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

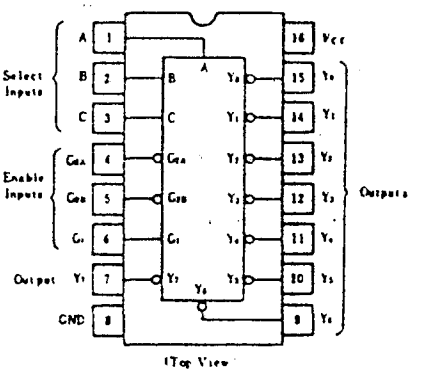
TRUTH TABLE

WE	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

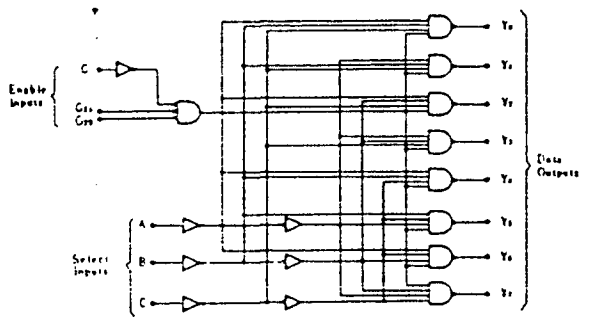
HD74LS138 ● 3-Line-to-8-Line Decoders/Demultiplexers

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An eanble input can be used as a data input for demultiplexing applications.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H; high level, L; low level, X; irrelevant
*; $G_2 = G_{2A} + G_{2B}$

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

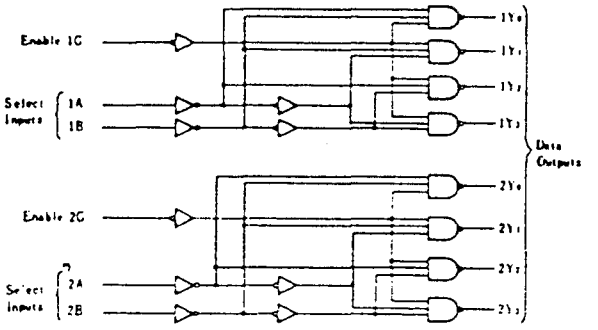
Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	V
Output voltage	V_{OH}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=−400μA		2.7	—	—	V
	V_{OL}	V_{CC}=4.75V, V_{IH}=2V, V_{IL}=0.8V	I_{OL}=4mA	—	—	0.4	V
			I_{OL}=8mA	—	—	0.5	
Input current	I_{IH}	V_{CC}=5.25V, V_I=2.7V		—	—	20	μA
	I_{IL}	V_{CC}=5.25V, V_I=0.4V		—	—	−0.4	mA
	I_I	V_{CC}=5.25V, V_I=7V		—	—	0.1	mA
Short-circuit output current	I_{OS}	V_{CC}=5.25V		−20	—	−100	mA
Supply current	I_{CC}	V_{CC}=5.25V, Outputs enabled and open		—	6.3	10	mA
Input clamp voltage	V_{IK}	V_{CC}=4.75V, I_{IN}=−18mA		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

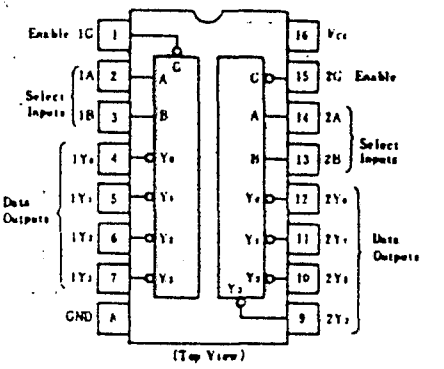
HD74LS139 ●Dual 2-line-to-4-line Decoders/Demultiplexers

The HD74LS139 comprises two individual two-line-to-four-line decoder in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs			Outputs			
Enable	Select					
G	B	A	Y_0	Y_1	Y_2	Y_3
H	×	×	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H; high level, L; low level, X; irrelevant

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−5	–	−42	mA
Supply current	I_{CC}	$V_{CC}=5.25V$, Outputs enabled and open		–	6.8	11	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

*$V_{CC}=5V$, $Ta=25°C$

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

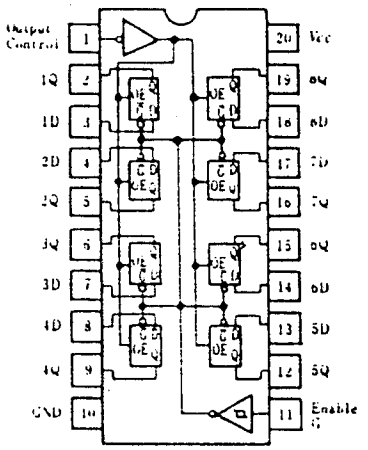
Item	Symbol	Inputs	Outputs	Levels of delay	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	Binary Select 1A, 1B 2A, 2B	1Y0~1Y3 2Y0~2Y3	2	$C_L=15pF$ $R_L=2k\Omega$	–	13	20	ns
	t_{PHL}					–	22	33	ns
	t_{PLH}			3		–	18	29	ns
	t_{PHL}					–	25	38	ns
	t_{PLH}	Enable 1G, 2G	1Y0~1Y3 2Y0~2Y3	2		–	16	24	ns
	t_{PHL}					–	21	32	ns

HD74LS373 ●Octal D-type Transparent Latches (with three-state outputs)

The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

■PIN ARRANGEMENT



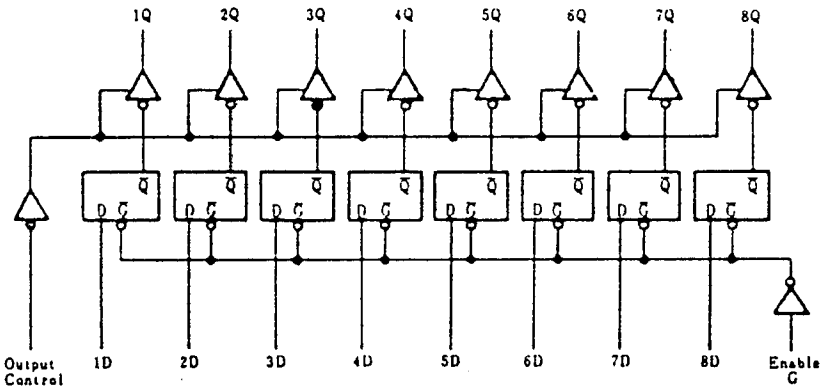
(Top View)

■FUNCTION TABLE

Inputs			Output
Output control	Enable G	D	Q
L	H	H	H
L	H	L	L
L	L	×	Q_0
H	×	×	Z

Notes: H = high level, L = low level,
X = irrelevant
Q_0 = level of Q before the indicated steady-state input conditions were established.
Z = off (high-impedance) state of a three-state output

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output voltage		V_{OH}	—	—	5.5	V
Output current		I_{OH}	—	—	−2.6	mA
		I_{OL}	—	—	24	mA
Enable pulse width	"H" level	t_w	15	—	—	ns
	"L" level		15	—	—	
Data setup time		t_{su}	5↓	—	—	ns
Data hold time		t_h	25↓	—	—	ns

Note) ↓ : The arrow indicates the falling edge of clock pulse.

BURR-BROWN®

INA101

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/√Hz at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST, TO-100, CERAMIC DIP AND PLASTIC PACKAGE

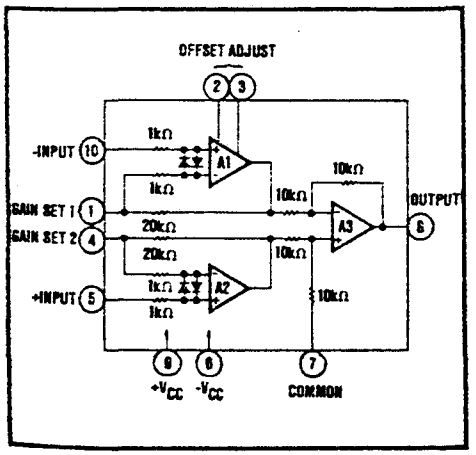
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

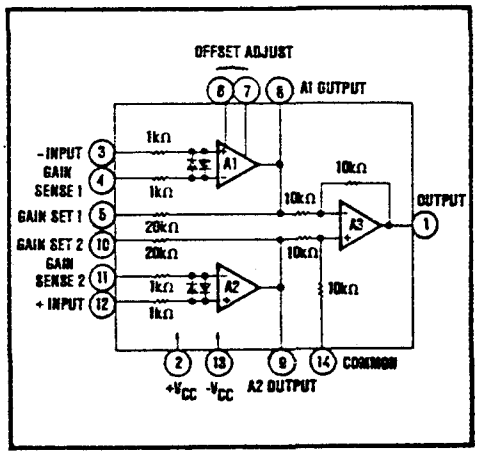
DESCRIPTION

The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected laser-trimmed thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.



M Package



G and P Packages

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	INA101AM/AG			INA101BM/BG			INA101CM/CG			INA101HP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN													
Range of Gain	1		1000	•		•	•		•	•		•	
Gain Equation		G=1+(40k/R_G)			•			•			•		V/V
Error From Equation, DC[1]		±(0.04+0.00016 −0.02/G)	±(0.1+0.0003G −0.05/G)		•	•		•	•		±(0.1+ 0.00015G) −0.05/G	±(0.3+ 0.0002G) −0.10/G	%
Gain Temp. Coefficient[2]													
G = 1		2	5		•	•		•	•		•	•	ppm/°C
G = 10		20	100		•	•		10	•		•	•	ppm/°C
G = 100		22	110		•	•		11	•		•	•	ppm/°C
G = 1000		22	110		•	•		11	•		•	•	ppm/°C
Nonlinearity, DC[2]		±(0.002+10^{-6}G)	±(0.005+2×10^{-6}G)		±(0.001 +10^{-6}G)	±(0.002 +10^{-6}G)		±(0.001 +10^{-6}G)	±(0.002 +10^{-6}G)		•	•	% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		•	•		•	•		•	•		V
Current	±5	±10		•	•		•	•		•	•		mA
Output Impedance		0.2			•			•			•		Ω
Capacitive Load		1000			•			•			•		pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		±(25+200/G)	±(50+400/G)		±(10+ 100/G)	±(25 +200/G)		±(10+ 100/G)	±(25+ 200/G)		±(125+ 450/G)	±(250+ 900/G)	µV
vs Temperature			±(2+20/G)			±(0.75 +10/G)			±(0.25+ 10/G)		±(2+20/G)		µV/°C
vs Supply		±(1+20/G)			•			•			•		µV/V
vs Time		±(1+20/G)			•			•			•		µV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30		±10	•		±5	±20		•	•	nA
vs Temperature		±0.2			•			•			•		nA/°C
vs Supply		±0.1			•			•			•		nA/V
Initial Offset Current		±15	±30		±10	•		±5	±20		•	•	nA
vs Temperature		±0.5			•			•			•		nA/°C
INPUT IMPEDANCE													
Differential		10^{10}||3			•			•			•		Ω||pF
Common-mode		10^{10}||3			•			•			•		Ω||pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		•	•		•	•		•	•		V
CMR with 1kΩ Source Imbal.													
DC to 60Hz, G=1	80	90		•	•		•	•		65	85		dB
DC to 60Hz, G=10	96	106		•	•		•	•		90	95		dB
DC to 60Hz, G=100 to 1000	106	110		•	•		•	•		100	105		dB
INPUT NOISE													
Input Voltage Noise													
f_o=0.01Hz to 10Hz		0.8			•			•			•		µV, p-p
Density, G=1000													
f_o=10Hz		18			•			•			•		nV/√Hz
f_o=100Hz		15			•			•			•		nV/√Hz
f_o=1kHz		13			•			•			•		nV/√Hz
Input Current Noise													
f_o=0.01Hz to 10Hz		50			•			•			•		pA, p-p
Density													
f_o=10Hz		0.8			•			•			•		pA/√Hz
f_o=100Hz		0.48			•			•			•		pA/√Hz
f_o=1kHz		0.35			•			•			•		pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness													
G = 1		300			•			•			•		kHz
G = 10		140			•			•			•		kHz
G = 100		25			•			•			•		kHz
G = 1000		2.5			•			•			•		kHz
Small Signal, ±1% Flatness													
G = 1		20			•			•			•		kHz
G = 10		10			•			•			•		kHz
G = 100		1			•			•			•		kHz
G = 1000		200			•			•			•		Hz
Full Power, G=1 to 100		5.4			•			•			•		kHz
Slew Rate, G=1 to 100	0.2	0.4		•	•		•	•		•	•		V/µs
Settling Time (0.1%)													
G = 1		30	40		•	•		•	•		•	•	µs
G = 100		40	55		•	•		•	•		•	•	µs
G = 1000		350	470		•	•		•	•		•	•	µs
Settling Time (0.01%)													
G = 1		30	45		•	•		•	•		•	•	µs
G = 100		50	70		•	•		•	•		•	•	µs
G = 1000		500	650		•	•		•	•		•	•	µs
POWER SUPPLY													
Rated Voltage		±15			•			•			•		V
Voltage Range	±5		±20	•		•	•		•	•		•	V
Current, Quiescent[5]		±6.7	±8.5		•	•		•	•		•	•	mA
TEMPERATURE RANGE[3]													
Specification	−25		+85	−55		+125	•		•		0	+70	°C
Operation	−55		+125	•		•	•		•		−25	+85	°C
Storage	−65		+150	•		•	•		•		−40	+85	°C

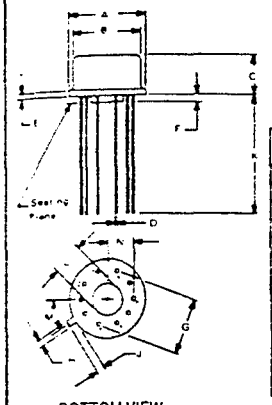
* Specifications same as for INA101AM/AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G. (4) Adjustable to zero at any one gain. (5) θ_{JC} output stage = 113°C/W, θ_{JC} quiescent circuitry = 19°C/W, θ_{CA} = 83°C/W.

MECHANICAL

M Package

TO-100



BOTTOM VIEW

Case = $-V_{CC}$

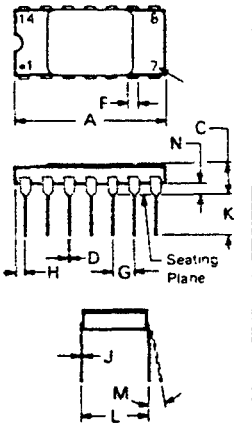
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane

Pin numbers shown for reference only
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
b	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

G Package

Hermetic DIP



Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.006	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	- -	10°	- -	10°
N	.009	.060	0.23	1.52

ORDERING INFORMATION

INA101 C G

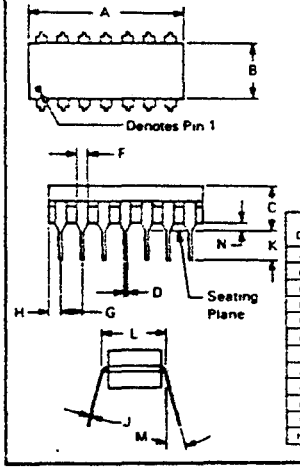
Basic Model Number

Performance Grade Code
- S: −55°C to +125°C
- A, C: −25°C to +85°C
- H: 0°C to +70°C

Package Code
- M: TO-100
- G: 14-Pin Hermetic DIP
- P: 14-Pin Plastic DIP

TO-100 (M Suffix)	Hermetic DIP (G Suffix)	Plastic DIP (P Suffix)
INA101AM	INA101AG	INA101HP
INA101CM	INA101CG	
INA101SM	INA101SG	

P Package



Case = $-V_{CC}$

Leads in true position within 0.10" (0.25mm) R at MMC at seating plane

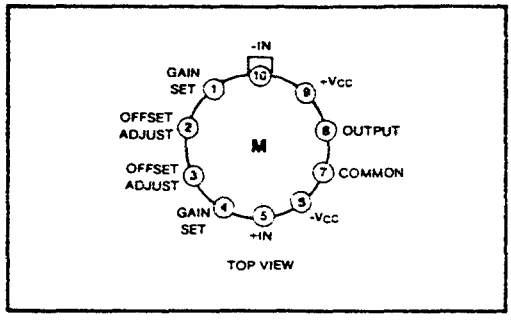
Pin numbers shown for reference only
Numbers may not be marked on package.

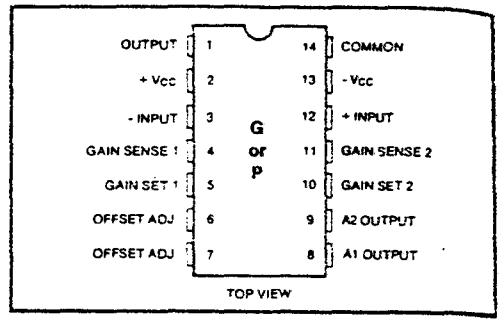
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C		.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095		
J	.008	.015	0.20	0.38
K	.100		2.54	
L	.300 BASIC		7.62 BASIC	
M		15°		15°
N	.020	.050	0.51	1.27

ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	$\pm V_{CC}$
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range:	
M, G	−65°C to +150°C
P	−40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration	Continuous to ground

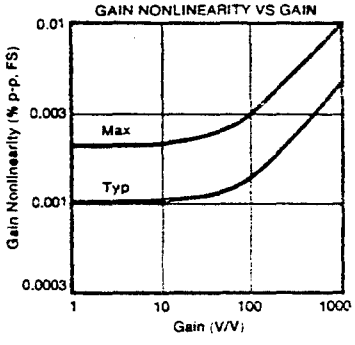
PIN CONFIGURATION

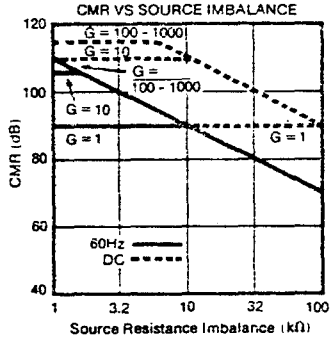


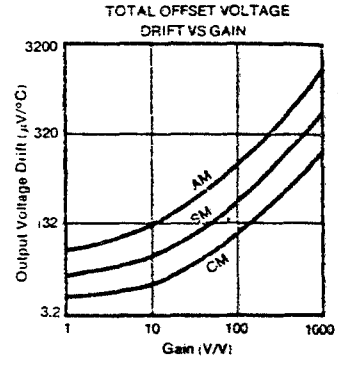


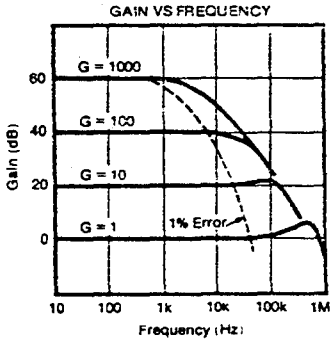
TYPICAL PERFORMANCE CURVES

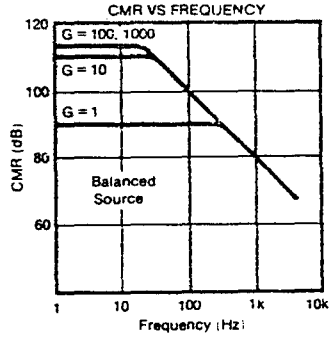
At +25°C and in circuit of Figure 2 unless otherwise noted.

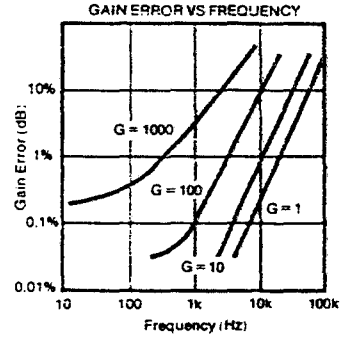


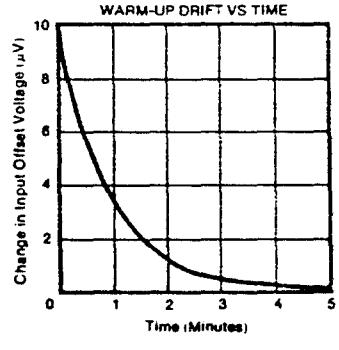


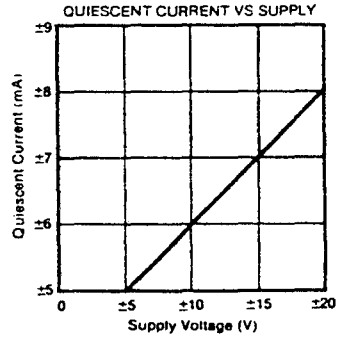


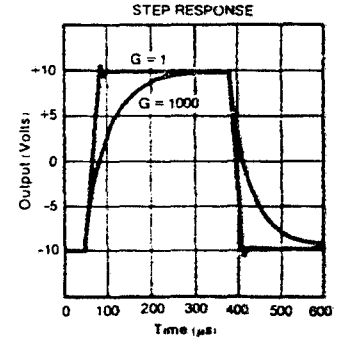


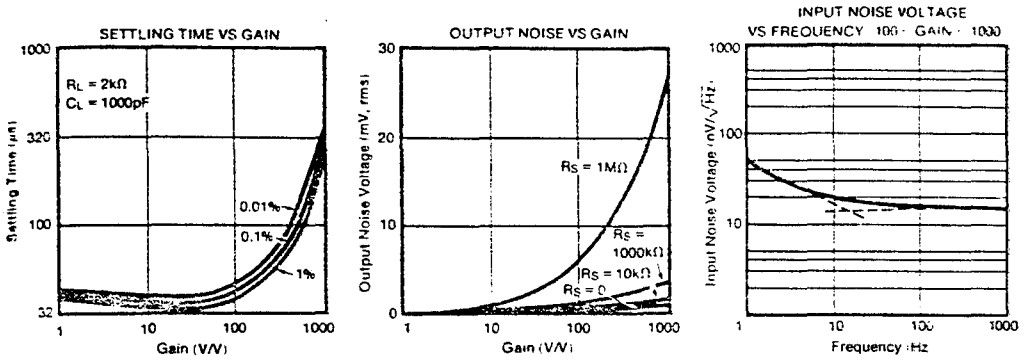












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

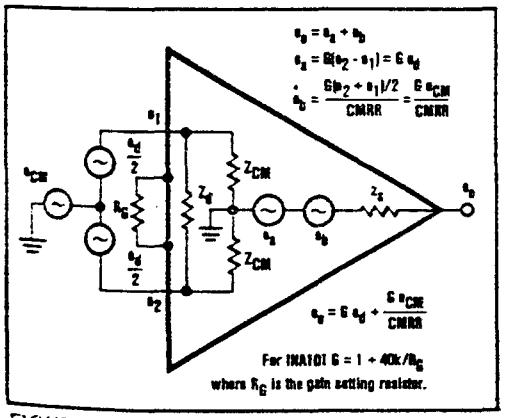


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

Simplified schematics of the INA101 are shown on the first page. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found in integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

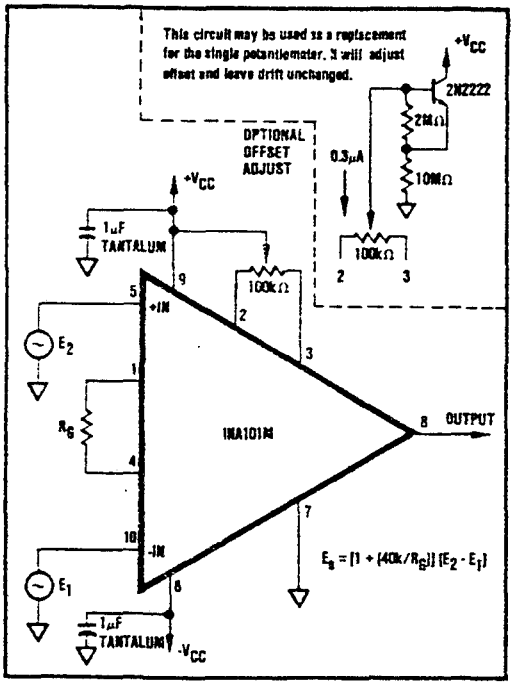


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately 0.31μV/°C per 100μV of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately ±10V or nonlinear operation will result.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 2) and occasionally that of the output (Figure 3). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 3 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2.

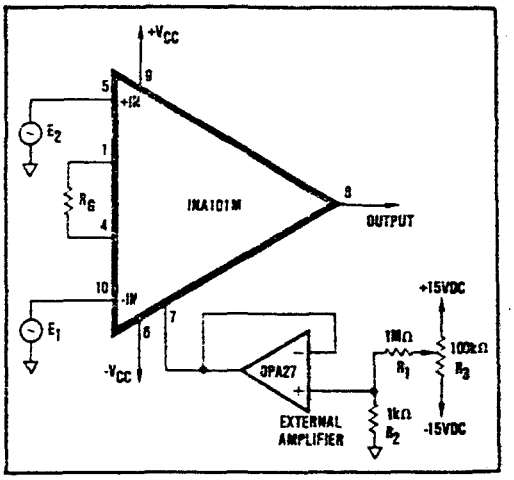


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

THERMAL EFFECTS ON OFFSET

To maintain specified offset performance, especially in high gain, prevent air currents from circulating around the input pins. This can be done by using a skirted heat sink on the INA101M package. Rapid changes in die temperature and thermocouple effects on the pins will then be minimized. Surrounding the package with low power components will also help to reduce air flow across the package and pins.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low level differential signals from

bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all of these with high precision.

Figures 4 through 16 show some typical applications circuits.

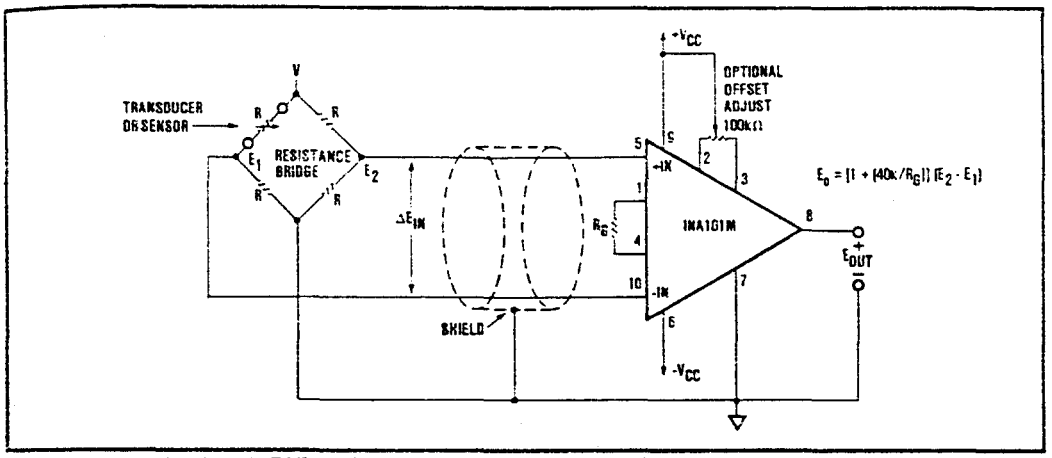


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

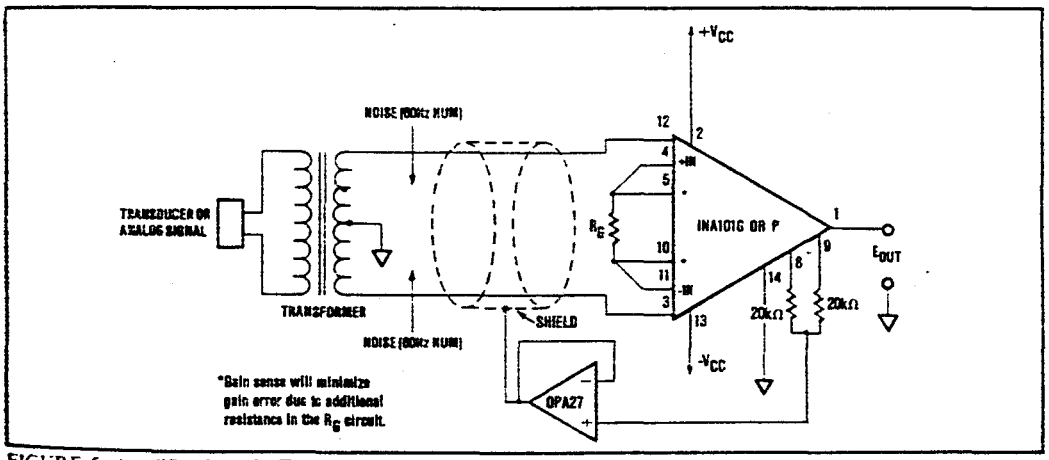


FIGURE 5. Amplification of a Transformer-Coupled Analog Signal.

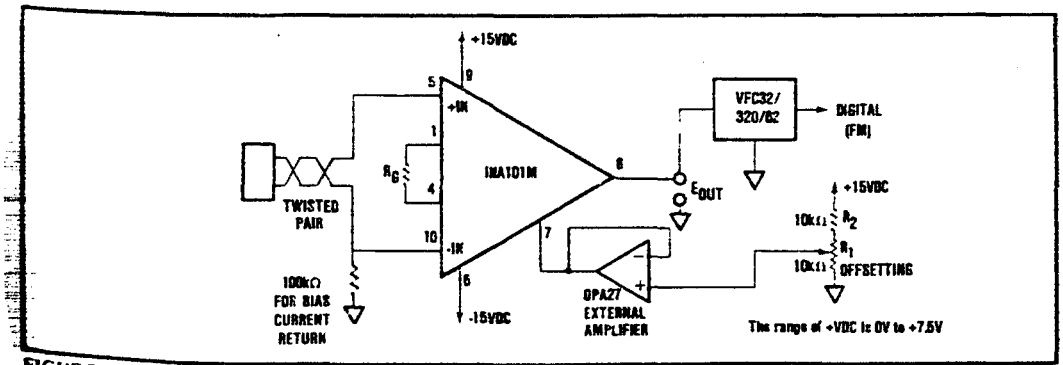


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

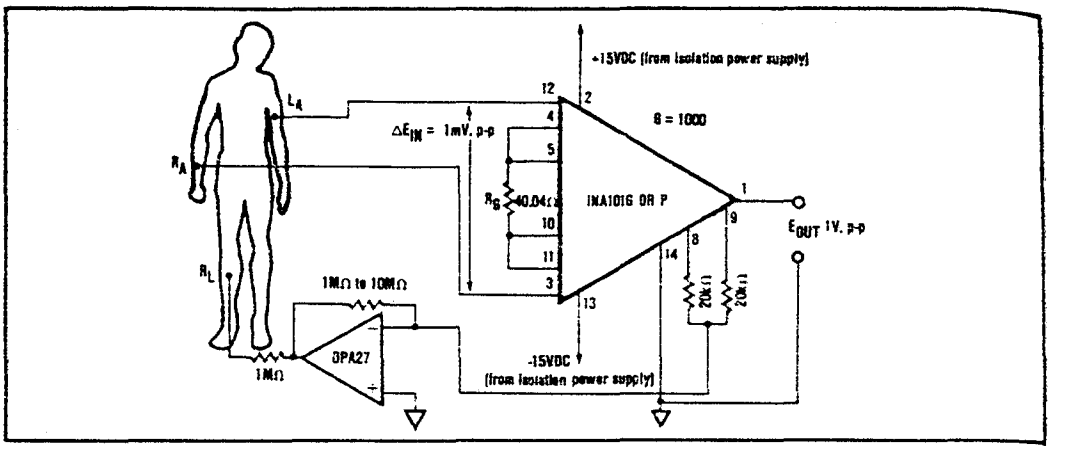


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

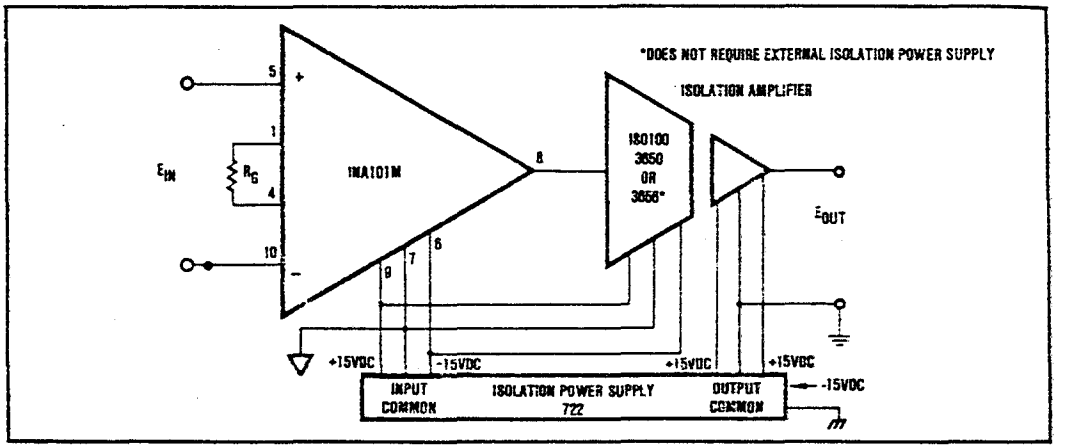


FIGURE 8. Precision Isolated Instrumentation Amplifier.

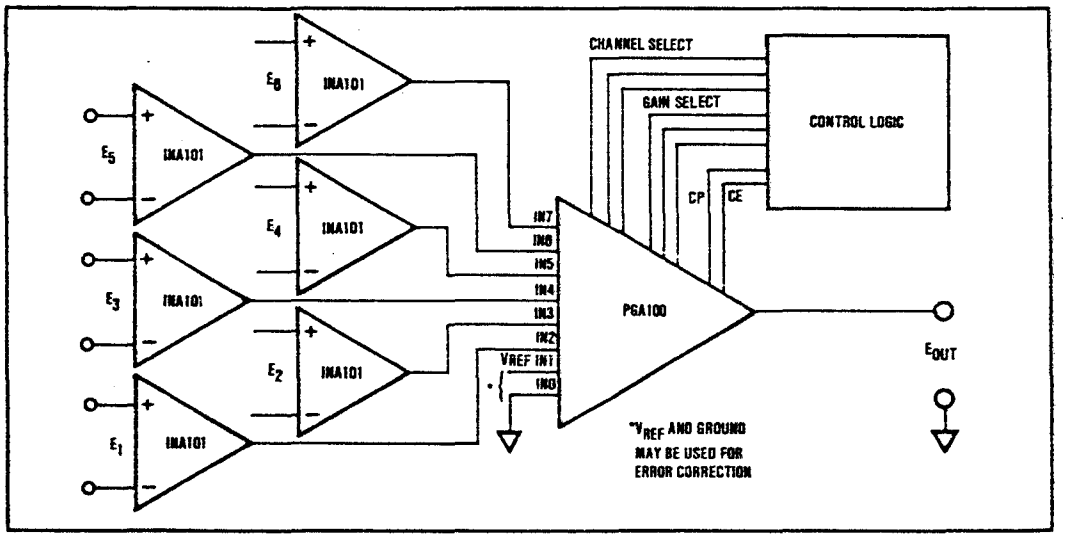


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

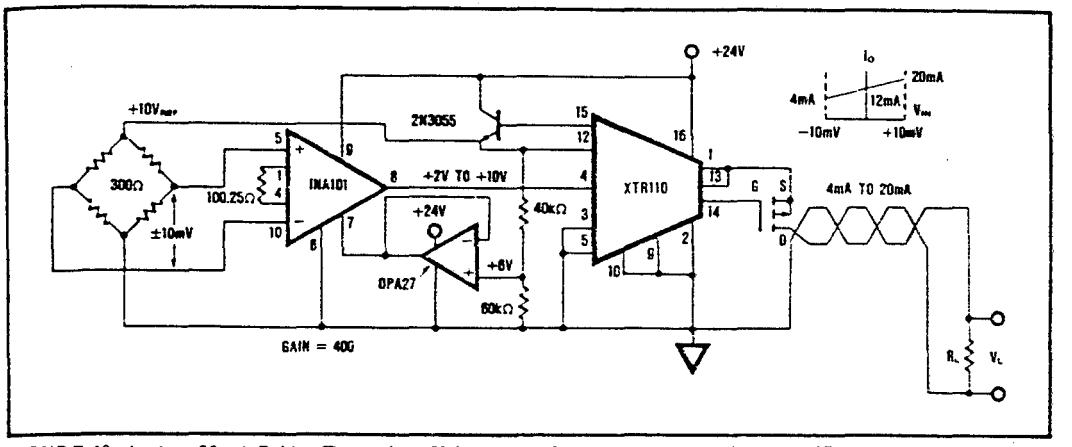


FIGURE 10. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

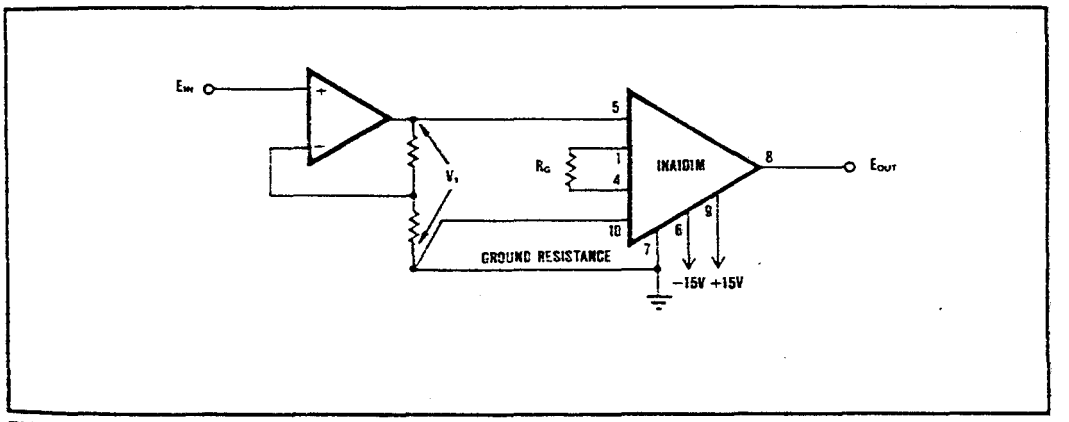


FIGURE 11. Ground Resistance Loop Eliminator (INA101 senses and amplifies V_1 accurately).

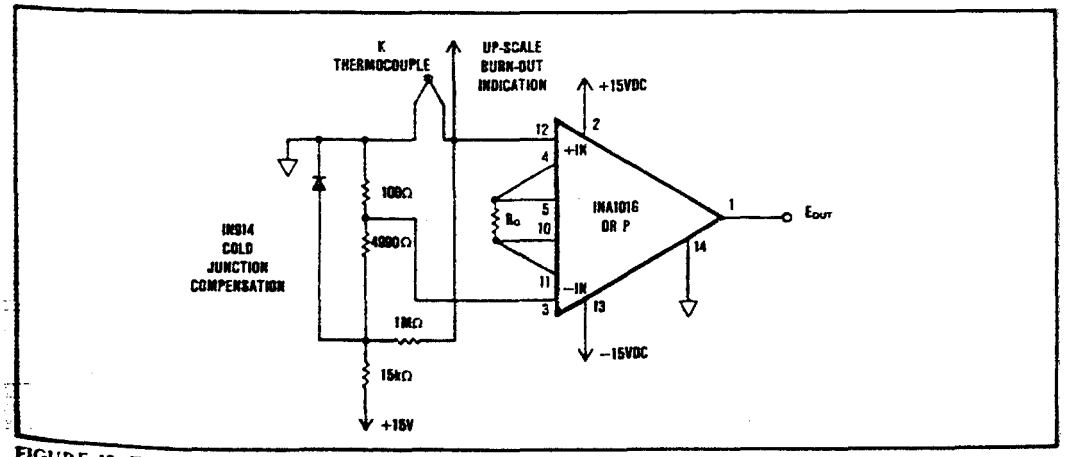


FIGURE 12. Thermocouple Amplifier with Cold Junction Compensation.

ICL7135
4½-Digit BCD Output A/D Converter

INTERSIL

GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDER-RANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

FEATURES

- **Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000 Volts Full Scale)**
- **Guaranteed Zero Reading for 0 Volts Input**
- **1pA Typical Input Current**
- **True Differential Input**
- **True Polarity at Zero Count for Precise Null Detection**
- **Single Reference Voltage Required**
- **Over-Range and Under-Range Signals Available for Auto-Range Capability**
- **All Outputs TTL Compatible**
- **Blinking Outputs Gives Visual Indication of Over-range**
- **Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Circuitry**
- **Multiplexed BCD Outputs**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7135CJI	0°C to +70°C	28-Pin CERDIP
ICL7135CPI	0°C to +70°C	28-Pin Plastic DIP
ICL7135EV/KIT	Evaluation Kit (PC Board, active, passive components)	

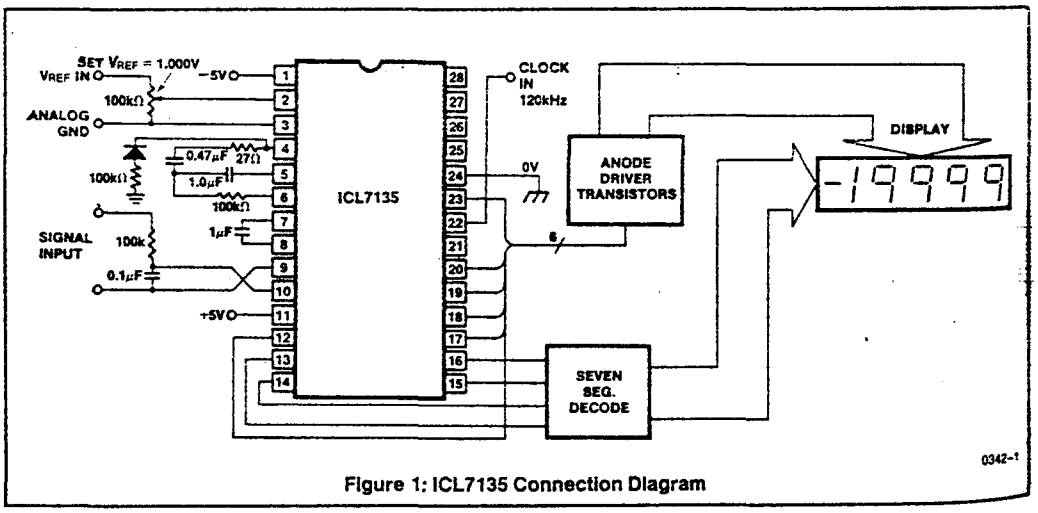


Figure 1: ICL7135 Connection Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

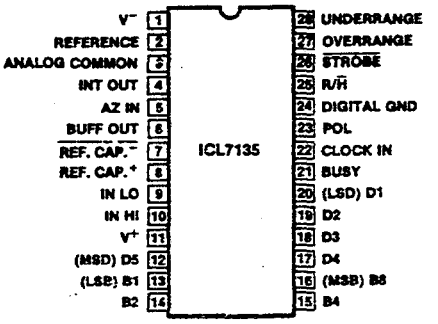
Supply Voltage V+ ..... +6V
V− ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Gnd to V+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0342-2

Figure 2: Pin Configuration
Outline dwgs JI, PI)

ELECTRICAL CHARACTERISTICS (Note 1)

$V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
ANALOG (Note 1) (Note 2)						
	Zero Input Reading	$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
	Ratiometric Reading (2)	$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
	Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leq V_{IN} \leq +2V$		0.5	1	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \leq V_{IN} \leq +2V$		.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error

NOTE: *All typical values have been characterized but are not tested.*

ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec) (Continued)

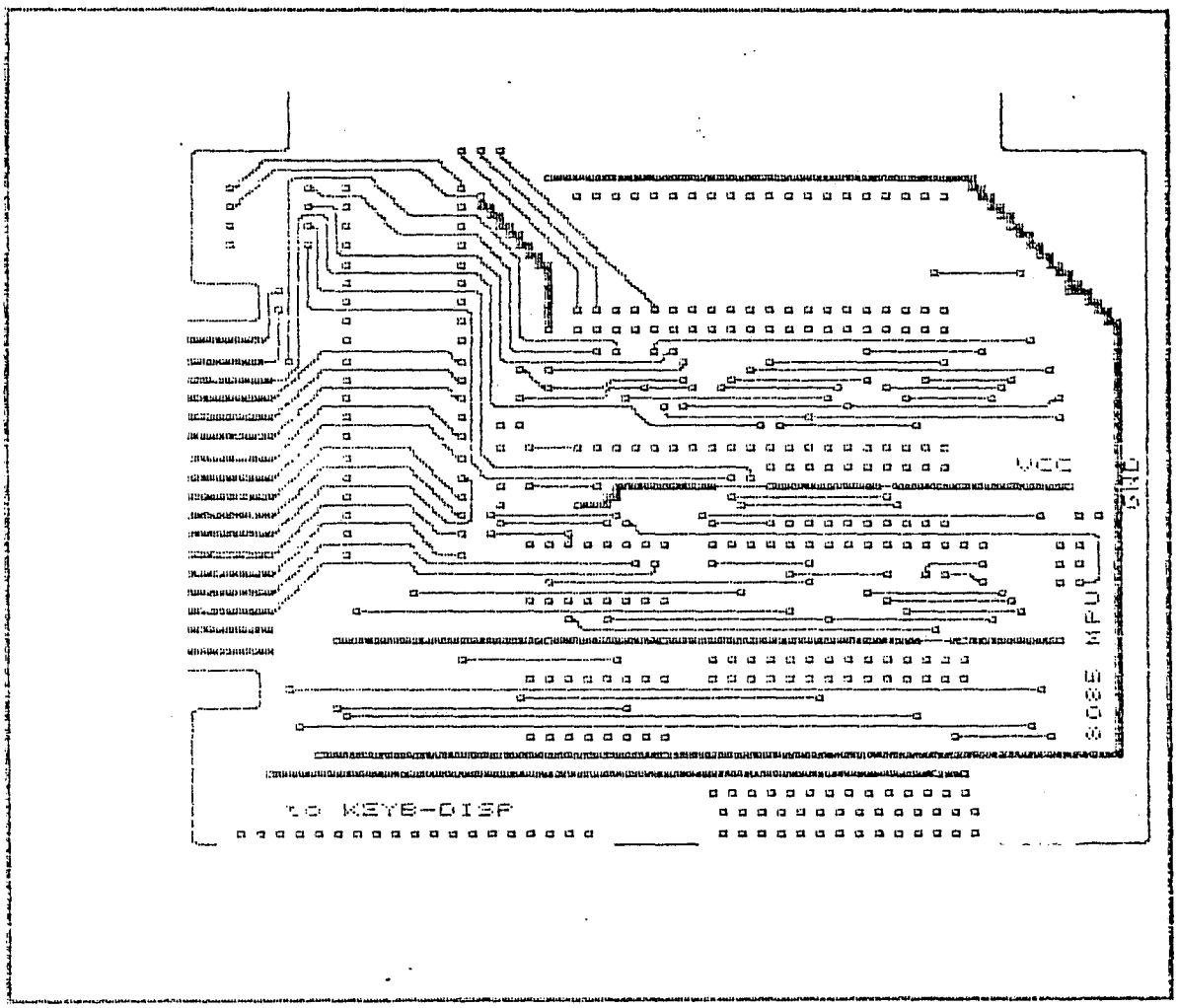
Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
e_n	Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
I_{ILK}	Leakage Current at Input	$V_{IN} = 0V$		1	10	pA
	Zero Reading Drift	$V_{IN} = 0V$ $0° \leq T_A \leq 70°C$		0.5	2	μV/°C
TC	Scale Factor Temperature Coefficient (3)	$V_{IN} = +2V$ $0 \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL						
INPUTS						
V_{INH}			2.8	2.2		V
V_{INL}				1.6	0.8	
I_{INL}	Clock in, Run/$\overline{Hold}$, See Figure 4	$V_{IN} = 0$		0.02	0.1	mA
I_{INH}		$V_{IN} = +5V$		0.1	10	μA
OUTPUTS						
V_{OL}	All Outputs	$I_{OL} = 1.6mA$		0.25	0.40	V
V_{OH}	B_1, B_2, B_4, B_8	$I_{OH} = -1mA$	2.4	4.2		V
V_{OH}	D_1, D_2, D_3, D_4, D_5 BUSY, $\overline{STROBE}$, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OH} = -10\mu A$	4.9	4.99		V
SUPPLY						
V^+	+5V Supply Range		+4	+5	+6	V
V^-	−5V Supply Range		−3	−5	−8	V
I^+	+5V Supply Current	$f_C = 0$		1.1	3.0	mA
I^-	−5V Supply Current	$f_C = 0$		0.8	3.0	
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF
CLOCK						
	Clock Freq. (Note 4)		DC	2000	1200	kHz

NOTES: 1. Tested in 4-½ digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.
2. Tested with a low dielectric absorption integrating capacitor and $R_{INT} = 0$. See Component Selection Section.
3. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" section for limitations on the clock frequency range in a system.

NOTE: All typical values have been characterized but are not tested

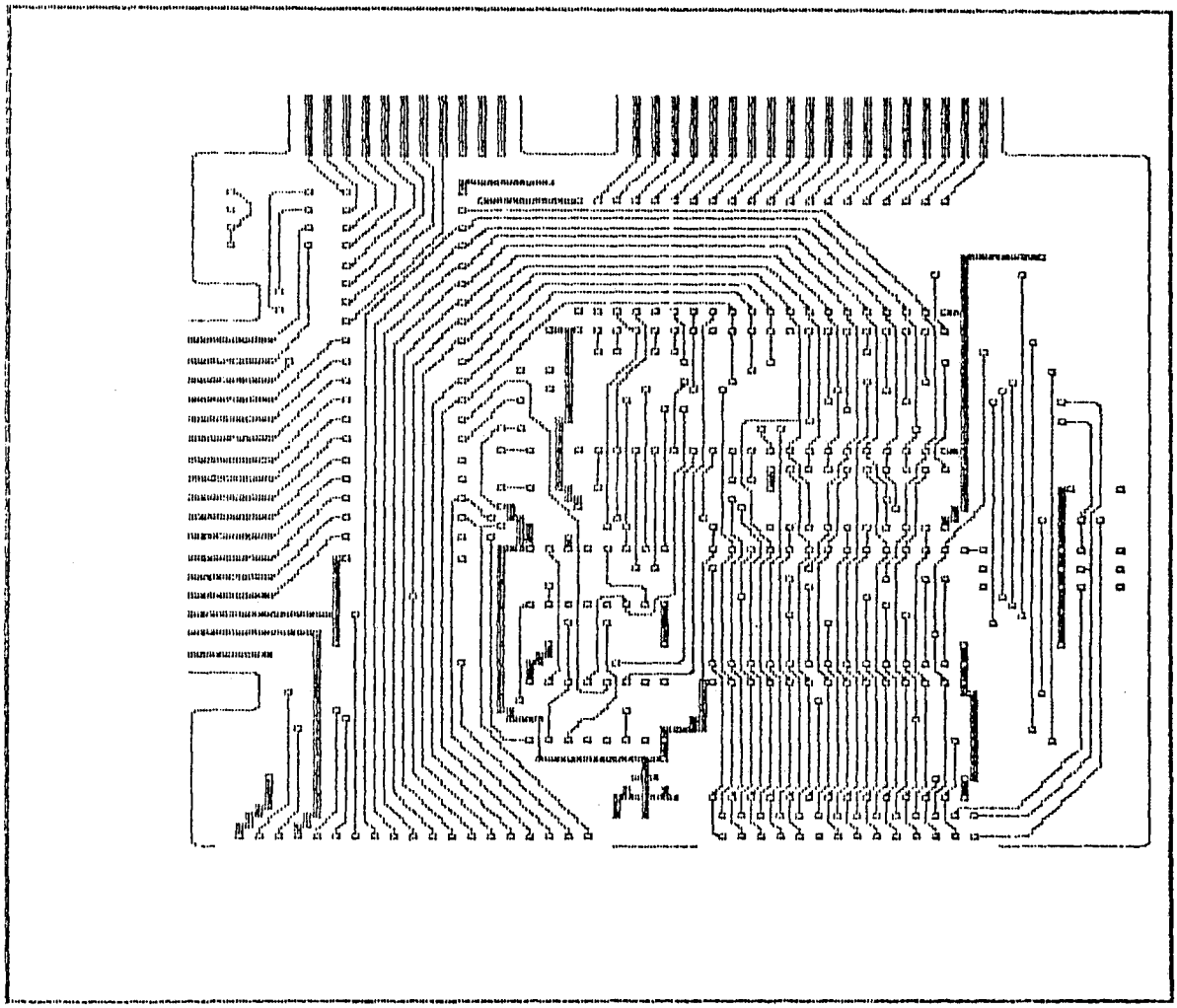
ЕК-3

1X checkplot 1 Jan 80 05:54:04
mp1.pcb
v1.4 r0 holes: 426 component side
approximate size: 5.85 by 5.00 inches



Mikroişlemci Devresinin Eleman Yüzü

1% checkplot 1 Jan 80 05:54:04
mpl.pcb
v1.4 r0 holes: 426 solder side
approximate size: 5.85 by 5.00 inches



Mikroişlemci Devresinin Lehim Yüzü

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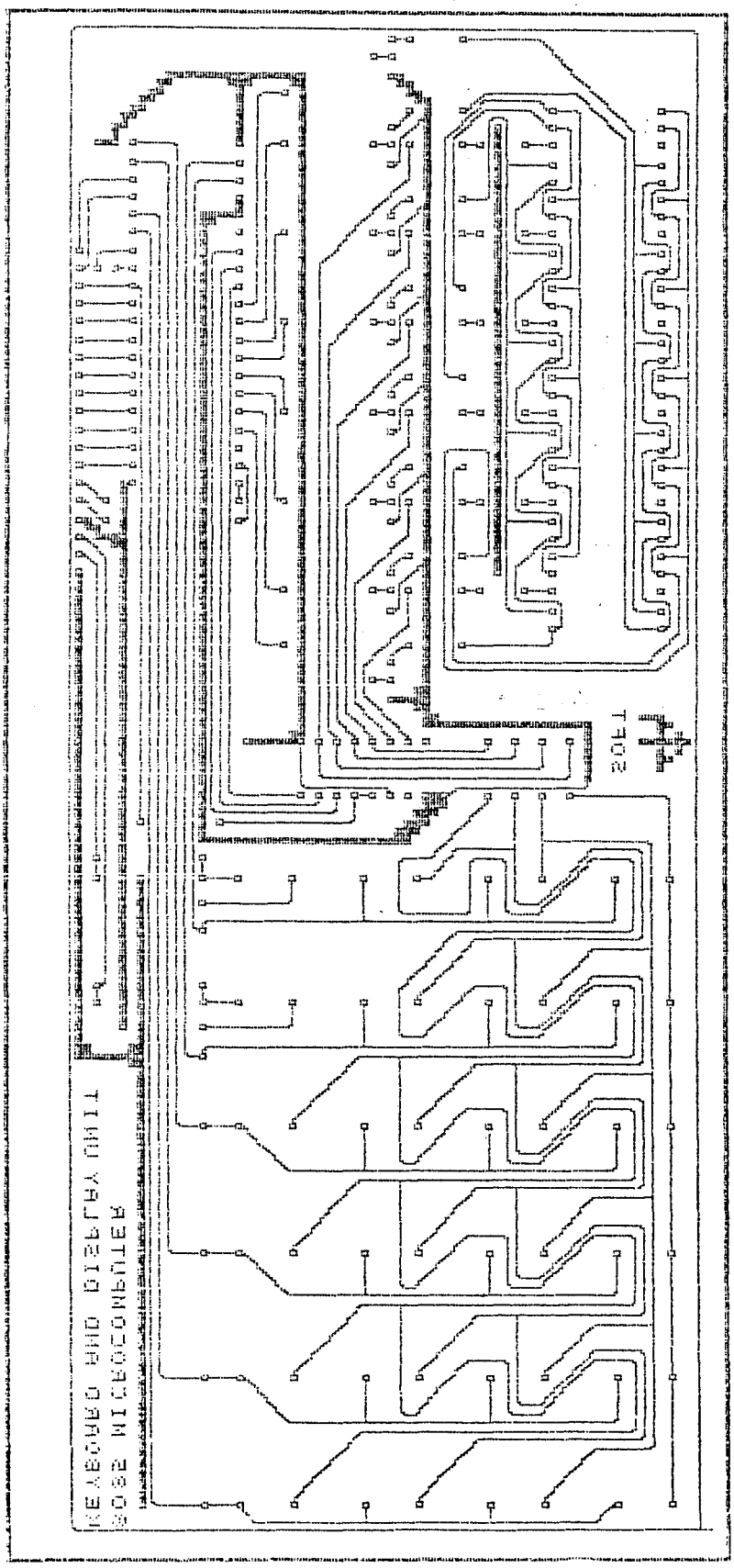
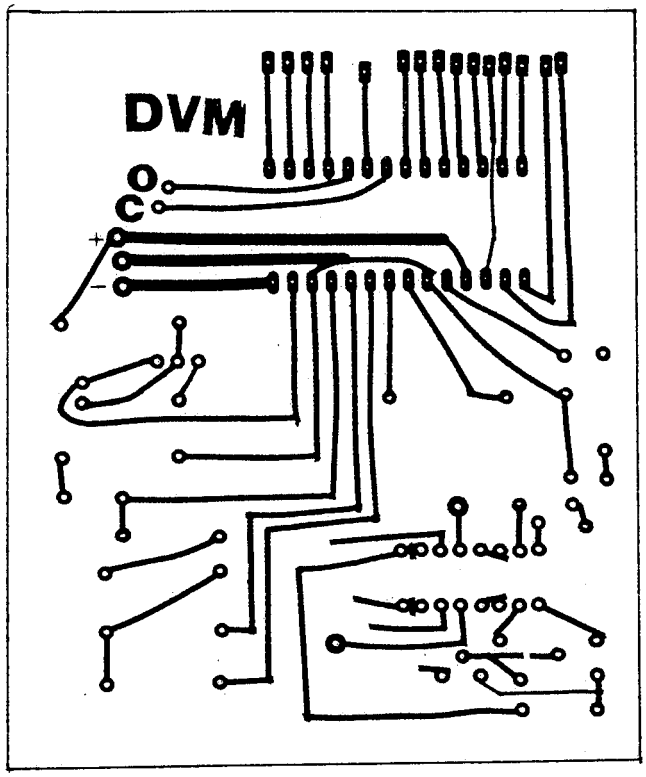
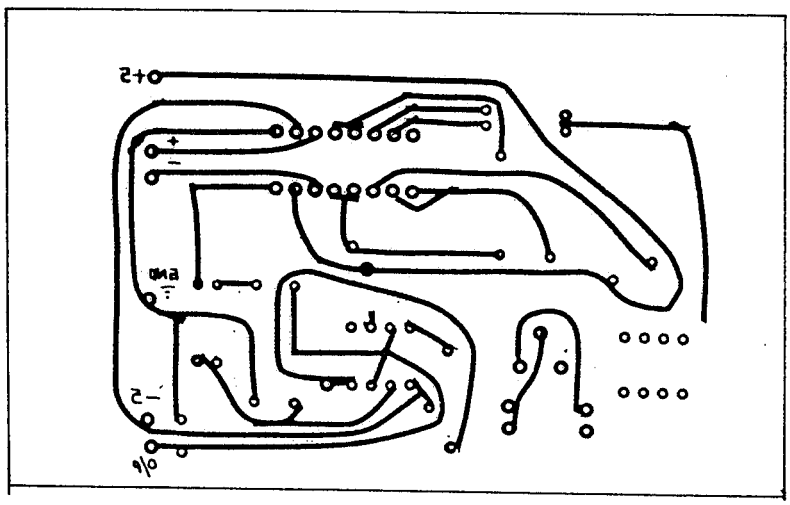
kd11.pcb
v1.4 r0 holes: 322 solder side
approximate size: 8.50 by 3.85 inches



Gösterge-Tuş Takımının Baskılı Devresi



DVM Kartının Baskılı Devresi



Kuvvetlendirici/Filtre Kartının Baskılı Devresi