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A DC~1.6 GHz DISTRIBUTED AMPLIFIER WITH GaAs MESFETs

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Abstract: In this study, a DC ~ 1.6 GHz bandwidth distributed amplifier (DA) is fabricated in printed circuit board (PCB). The scattering (S-) parameters of the distributed amplifier are measured and compared with simulated results. In characterization of the amplifier, small-signal microwave S-parameters given at some discrete frequencies of transistors are utilized. According to obtained results, it is observed that measured and simulated results are in relatively good agreement.

Keywords: Distributed amplifier, broadband, S-parameters, PCB fabrication.

DC~1.6 GHz GaAs MESFET'lere sahip Dağılmış Parametreli Kuvvetlendirici

Öz: Bu çalışmada, DC ~ 1.6 GHz bant genişliğine sahip bir dağılmış parametreli kuvvetlendirici (DA) baskı devre kartında gerçeklenmiştir. Dağılmış parametreli kuvvetlendiricinin performans parametreleri olan saçınım (S-) parametreleri ölçülmüş ve sonuçlar benzetim sonuçlarıyla kıyaslanmıştır. Yükselticinin karakterizasyonunda, devrenin aktif elemanları olan transistörlerin bazı frekanslarda verilmiş küçük-işaret mikrodalga S-parametreleri ve pasif elemanların değerleri kullanılmıştır. Elde edilen sonuçlara göre, ölçülen ve benzetilen sonuçlar nispeten uyumludur.

Anahtar Kelimeler: Dağılmış parametreli kuvvetlendirici, Genişbant, S-parametreleri, PCB gerçekleme.

1. INTRODUCTION

In many communication systems, transmitters have to provide a certain gain in a very wide frequency range. Distributed amplifiers (DAs) or traveling wave amplifiers (TWAs) are one of the efficient ways to obtain flat gain, linear phase, and low return loss over a wide frequency band. In recent years, distributed amplifiers are implemented by using Gallium Arsenide Metal Semiconductor Field Effect Transistors (GaAs MESFETs) and Monolithic Microwave Integrated Circuit (MMIC) technology. In literature, many workers have reported DAs with several design considerations and especially focused on increasing the gain-bandwidth product and the gain flatness, as well as output capabilities. In some of these studies, 9 dB gain an ±1 dB gain flatness in the 1-13 GHz frequency band (Ayaslı and others, 1982), 6 dB gain with 2 GHz bandwidth (Jutzi, 1969), 7 dB gain with 112 GHz bandwidth (Agarwal and others, 1998), 5 dB gain with 157 GHz bandwidth (Agarwal and others, 1998), 5 dB gain with 180 GHz bandwidth

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(Agarwal and others, 1998) are obtained. In (Eriksson and others, 2015), the two-cascaded single-stage DA design exhibited an average gain of 16 dB from 2 to 237 GHz. In this study, authors stated that the bandwidth obtained is the largest bandwidth for amplifiers reported so far in any technology. In (Narendra and others, 2013), gain of 10 dB covering a bandwidth from 100 – 800 MHz is implemented for Software Defined Radio (SDR) applications. Furthermore, DA structure has found several other circuit applications such as power combiner and splitter (Levy and others, 1986), circulator (Leisten and Collier, 1988), active frequency multiplier (Pavio and others, 2008), active mixer (Tang and Aitchison, 1985), active impedance transformer (Cioffi, 1989), and multidecade oscillator (Skvor and others, 1992).

For analysis and design of DA, analytical and graphical methods have been developed in which the performance of the amplifiers are evaluated by using analytical expressions as explained in (Aitchison, 1985), (Beyer and others, 1984), (Ayaslı and others, 1982). In addition, distributed amplifiers have been also analyzed and designed with a computer simulation using sophisticated models of transistor developed from measured S-parameters (Niclas and others, 1983), (Niclas and others, 1983), (Strid and Gleason, 1982).

In (Hiçdurmaz and Özzaim, 2011), a DC-1.6 GHz distributed amplifier was designed by using Microwave Office as a computer aided design (CAD) simulator. In this paper, the implementation of the designed circuit using discrete MESFET devices (NE34018 Gallium Arsenide HJ-FET) is presented, and the simulated and measured results are compared to gain insight into the practical aspects of the distributed amplifiers.

2. DISTRIBUTED AMPLIFICATION THEORY

Conventionally, DA is associated with two artificial transmission lines as shown in Figure 1.

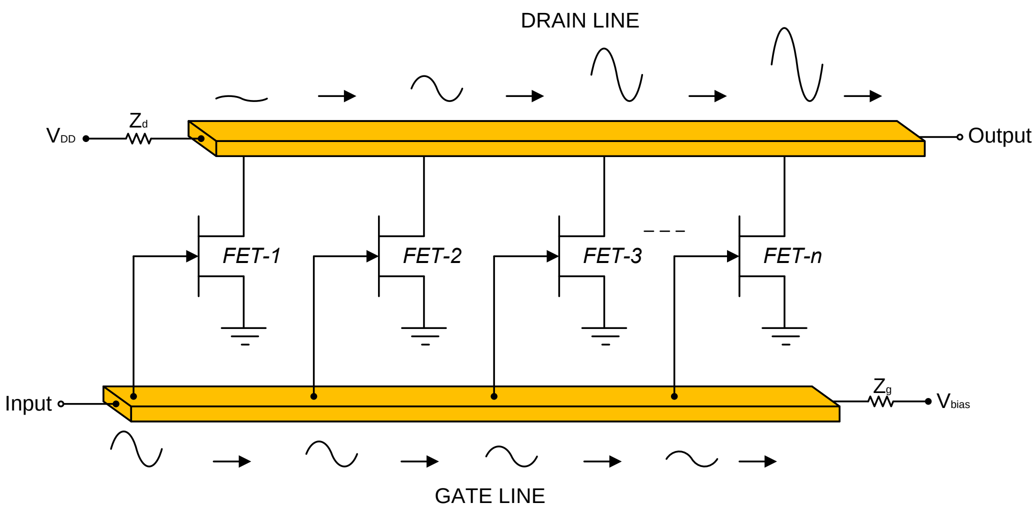

Figure 1:
The concept of conventional n- stage DA (Kumar and Grebennikov,2015)

As one of these lines makes up the input gate line, the other forms the drain output line. Basically artificial lines consists of series inductance and shunt capacitances. Thus, two constant-k transmission lines which have different cut-off frequencies and attenuation characteristics are obtained. While the shunt capacitors of the gate line are provided by the gate capacitance C_{gs} of the FETs, the drain-line shunt capacitors are provided by the FETs drain capacitance C_{ds}. Lengths of transmission line are utilized to make up the series inductances (Pozar, 2012).

In DA, input signal propagates through the gate line by contacting each FET. The input voltage that comes into view at the gate of each FET is increased by the FET's transconductance, producing current in the drain line. For producing the gain, it is necessary that these drain currents add in phase while the signal propagates throughout the drain line toward the output of DA. In that case, the phase shift between FETs along the drain line must be exactly the same as the phase shift between FETs along the gate line. This is achieved by carefully choosing the propagation constants and lengths of the gate and drain lines for constructive phasing of the output signals. The termination impedances, Z_g and Z_d on the transmission lines are used to absorb waves traveling in the reverse directions. Z_g and Z_d are matched to characteristic impedance of gate line and drain line, respectively, to avoid reflections. Since the lines are severely loaded by the FETs' resistances, the number of active device to be used is limited. Because the attenuation along the transmission lines will eventually exceed the gain obtained by adding an additional active device (Pozar,2012).

The forward gain of a DA which includes n active devices can be derived from simplified equivalent circuit model of DA described in Figure 2. The gate and drain channels of FETs have parasitic reactance C_{gs} and C_{ds}, respectively. The feedback capacitance C_{gd} can be usually ignored for simplification. The transconductance g_m is a voltage-controlled current source that governs the magnitude of the current flowing through the device. The transconductance is controlled by the voltage V_{gs} across capacitance C_{gs}.

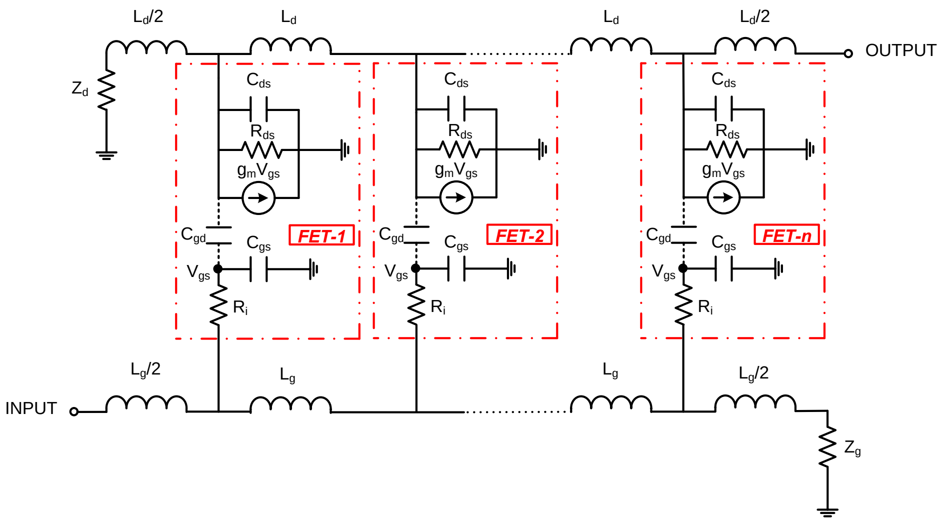

Figure 2:
Simplified Equivalent Model of DA with n-stages (Virdee and others,2004)

If DA circuit is considered to have loss-free components, then the forward available gain G can be given as (Pozar,2012)

$$G = \frac{1}{4} g_m^2 n^2 Z_d Z_g \tag{1}$$

This expression shows that the gain can be increased without limit by increasing the number of FETs on the same bandwidth. Unfortunately, in implementation the gain of DA does not increase with n due to losses in lines. This is because, a more accurate gain expression is given by (Pozar,2012)

$$G = \frac{1}{4} g_m^2 Z_d Z_g \left[\frac{e^{-A_g n} - e^{-A_d n}}{A_g - A_d} \right]^2 \tag{2}$$

where A_g and A_d are the gate- and the drain-line attenuation factors, respectively and the expressions for these factors are defined by

$$A_g = \frac{\left(\frac{f_c}{f_g}\right)\left(\frac{f}{f_c}\right)}{\sqrt{\left\{1-\left[1-\left(\frac{f_c}{f_g}\right)^2\right]\left(\frac{f}{f_c}\right)^2\right\}}} \tag{3}$$

$$A_d = \frac{\left(\frac{f_d}{f_c}\right)}{\sqrt{\left\{1-\left(\frac{f}{f_c}\right)^2\right\}}} \tag{4}$$

where f_g, f_d and f_c are the gate-circuit cut-off frequency, the drain-circuit cut-off frequency and the cut-off frequency of the lines, respectively. These values are taken as

$$f_g = \frac{0.5}{\pi R_i C_{gs}} \tag{5}$$

$$f_d = \frac{0.5}{\pi R_{ds} C_{ds}} \tag{6}$$

$$f_c = \frac{1}{\pi\sqrt{L_g C_{gs}}} = \frac{1}{\pi\sqrt{L_d C_{ds}}} \tag{7}$$

The optimum number of FETs, N_{opt} that maximizes gain at a given frequency is expressed as (Pozar,2012)

$$N_{opt} = \frac{\ln\frac{A_d}{A_g}}{A_d - A_g} \tag{8}$$

From these expression, it seems that in order to characterize a DA, an accurate small signal model of FET is essential. Equivalent circuit parameter values of a FET can be extracted using given set of S-parameter. A number of ways to do this are given in studies of (Berroth and Bosch, 1990) and (Kondoh, 1986).

In (Hiçdurmaz and Özzaim, 2011), the design and performance prediction of DA was performed by using CAD simulator and microwave S-parameter data of FET provided by the manufacturer at a single specified bias.

3. BIAS CIRCUIT of GaAs FETs

The DC bias circuit of the designed DA is shown in Figure 3. This circuit requires a bipolar power source. To prevent transient burnout of the GaAs FETs during turn-on, it is firstly applied a negative bias to the gate (i.e. $V_g < 0$) and then applied the drain voltage ($V_d > 0$). Thus, the FETs are safely operated (Gonzalez, 1997).

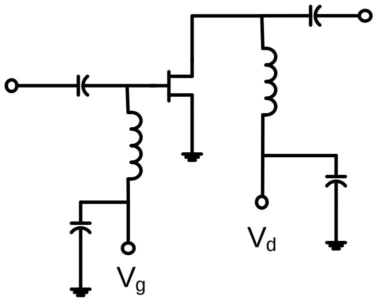

Figure 3:
The DC bias circuit of the designed DA (Gonzalez, 1997)

In designed bias circuit, it was used inductors of 100 nH as RF chokes and bypass capacitor of 1 nF. The quiescent point of FETs was selected as V_{ds} = 2 V and I_d = 10 mA.

4. MICROSTRIP LINES

Microstrip lines are utilized commonly in constructing microwave transistor amplifiers since they are easily fabricated using printed-circuit techniques. The placement of lumped elements and transistors can be easily made on metal surface of them. The geometry of a microstrip line is given in Figure 4.

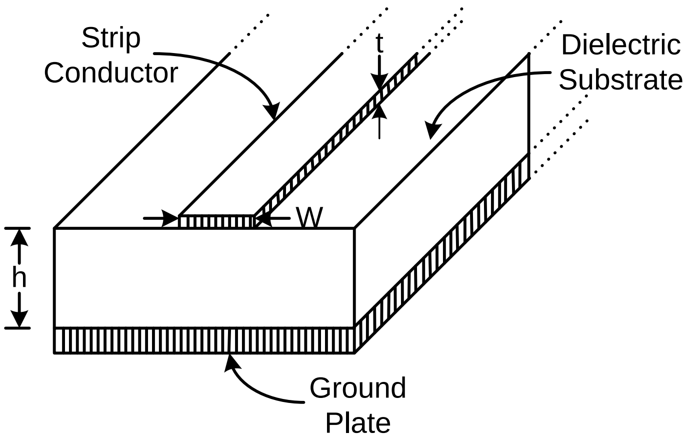

Figure 4:
Microstrip geometry (Gonzalez, 1997)

Assuming negligible thickness of the strip conductor (i.e. t/h ≤ 0.005), the expressions relating to characteristic empedance Z_0 and relative permeabilite ε_r to the ratio W/h of the microstrip line are as follows (Gonzalez, 1997):

For $W/h \leq 2$:

$$\frac{W}{h} = \frac{8e^{A}}{e^{2A} - 2} \tag{9}$$

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \tag{10}$$

For $W/h \geq 2$:

$$\frac{W}{h} = \frac{2}{\pi}\left\{B - 1 - \ln(2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r}\right]\right\} \tag{11}$$

where

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}} \tag{12}$$

The designed DA with CAD simulator in (Hiçdurmaz and Özzaim, 2011) was realised by microstrip lines since they were more suitable for implementation.

5. DA CIRCUIT FABRICATION

The designed DA layout made by Protel DXP layout designer program is shown in Figure 5. In here, the elements of the DA circuit were suitably drawn according to their dimensions.

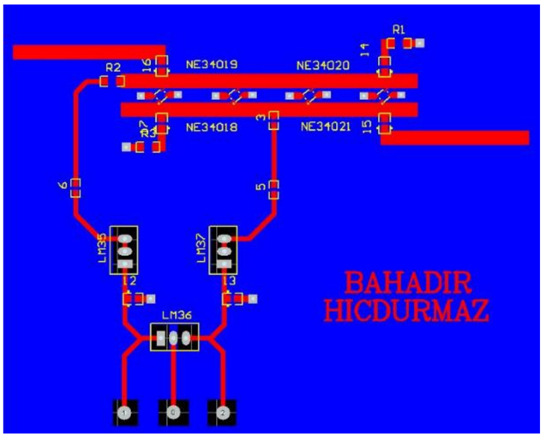

Figure 5:
PCB layout of the designed DA

The selection of PCB substrate is very important. Because, it should be able to respond to the operation over frequency band of the DA. With this aim, Rogers RO 4003 substrate was selected. This substrate has relative a permittivity ε_r of 3.38, dielectric thickness h of 1.52 mm and loss tangent (i.e. tan δ) of 0.0027. The realized circuit of DA is given in Figure 6.

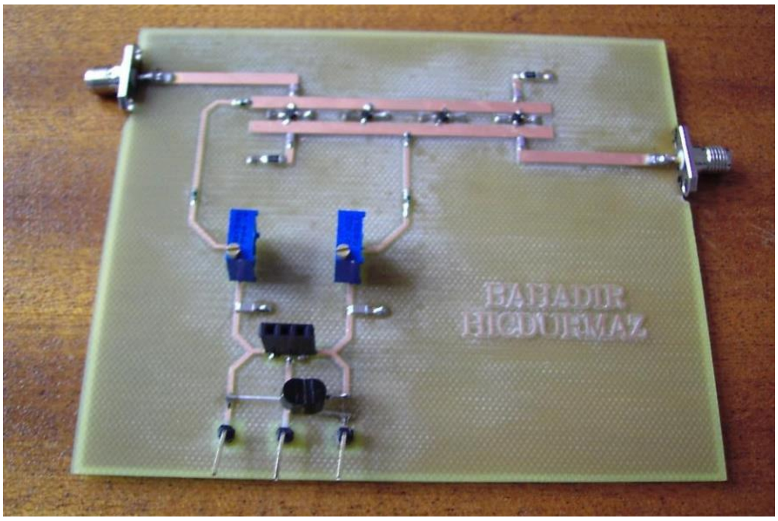

Figure 6:
The realized PCB circuit of DA

6. PERFORMANCE EVALUATION of DA

S-parameters of the realized DA were measured by using a network analyzer device over frequency range of 500 MHz to 3 GHz. Measured and simulated S-parameter results of designed DA are compared in Figure 7 – 11. Measured and simulated gain parameters, $|S_{21}|_{dB}$ data are given in Figure 7. From here, it is shown that measured $|S_{21}|_{dB}$ data are approximately 45-50 % less than simulated $|S_{21}|_{dB}$ data and measured 3-dB bandwidth is DC~1.6 GHz while simulated one is DC~2.5 GHz.

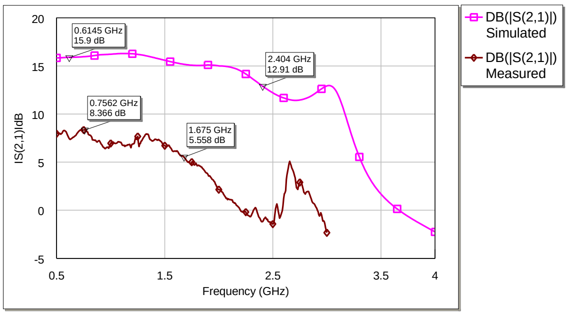

Figure 7:
Measured and simulated $|S_{21}|_{dB}$ data

Measured and simulated return loss parameters, $|S_{11}|_{dB}$ and $|S_{22}|_{dB}$ data are given in Figure 8 and Figure 9, respectively. It is clear that the obtained results are relatively matched. On the other hand, although the measured results is not better than the simulated ones, the resultant circuit can be relatively used over the frequency band of operation.

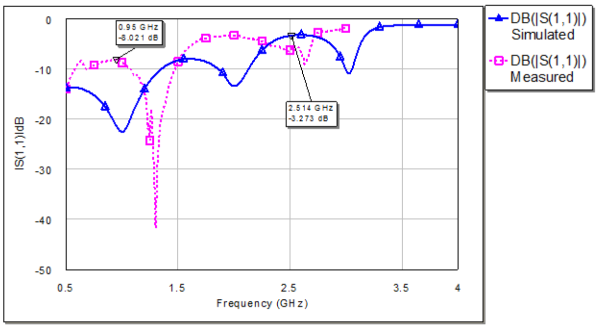

Figure 8:
Measured and simulated $|S_{11}|_{dB}$ data

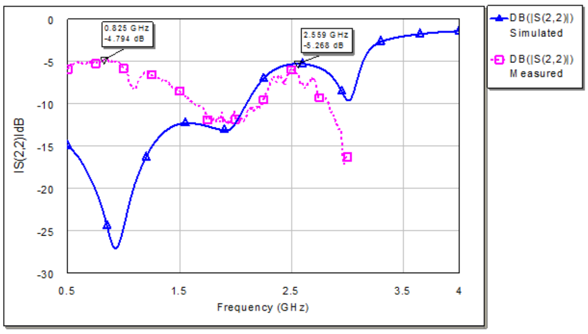

Figure 9:
Measured and simulated $|S_{22}|_{dB}$ data

Figure 10 shows measured and simulated output isolation parameters, $|S_{12}|_{dB}$ which are relatively matched. It is shown that the isolation of the realized circuit is quite good over operation frequency band ($|S_{12}|_{dB} < -20$ dB).

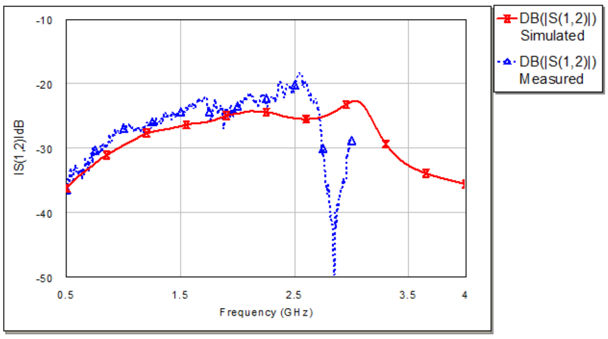

Figure 10:
Measured and simulated $|S_{22}|_{dB}$ data

The measured and simulated phases of S_{21} are given in Figure 11. It is shown that the linearity of the realized circuit is relatively good over operation frequency band.

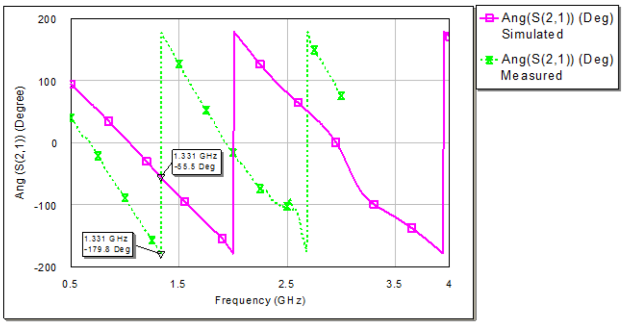

Figure 11:
Measured and simulated $(S_{21})_{Ang}$ data

As explained above, some differences between measured and simulated results were reported. The main reason of these differences is that PCB construction is not suitable enough to compare to MMIC construction for this circuit. Probably, in PCB, parasitic coupling between different parts of circuit has occurred and hence DA's overall performance has been degraded. Furthermore, the used simulation tool could not predict undesired coupling between the circuit elements.

7. CONCLUSION

In this paper, a DC ~ 1.6 GHz DA with approximately 8.35-dB gain has been achieved. The measured S- parameters of DA have been compared with simulated results. It was demonstrated that measured and simulated results were relatively matched. This DA circuit can find several application areas such as pre-amplifiers in radio or television communications.

As a result, the DA which is one of the most popular broadband amplifiers nowadays is realized. With the experience gained in this work, it is expected that MMIC implementation studies can made more accurately in a future design.

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